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SCOPES: MORE THAN MEETS THE EYE

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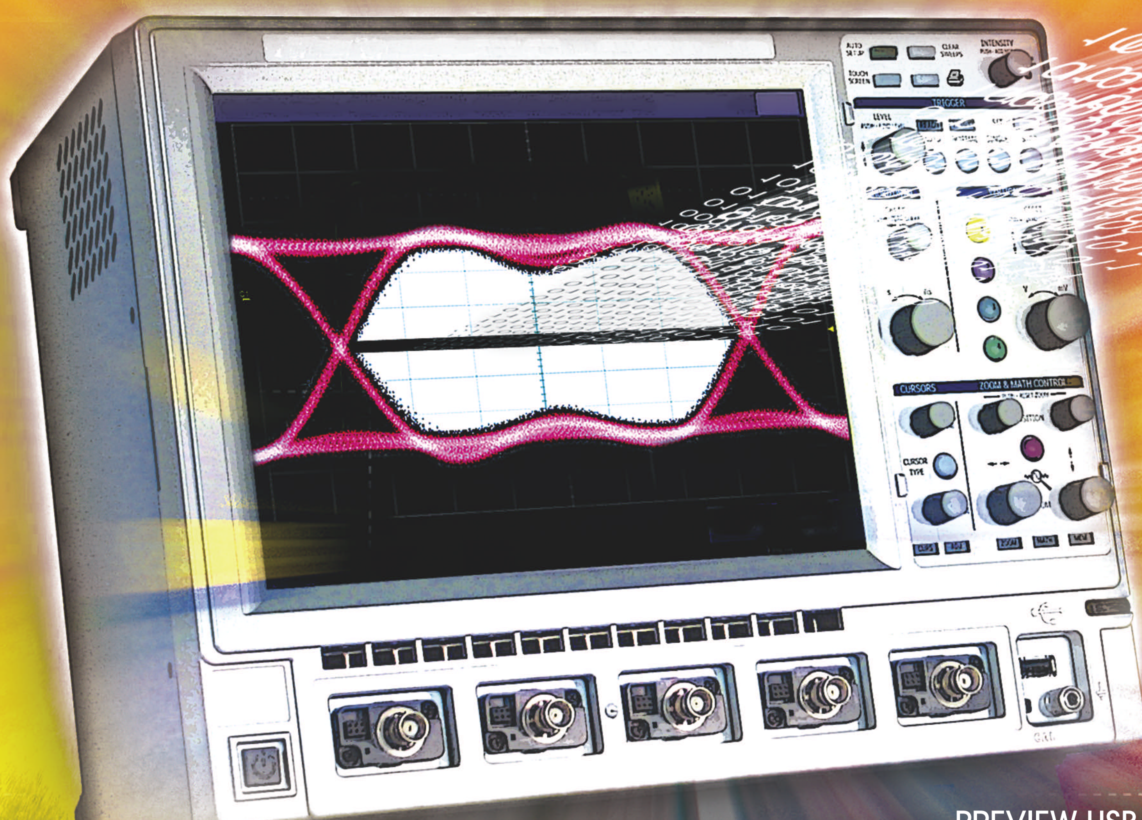

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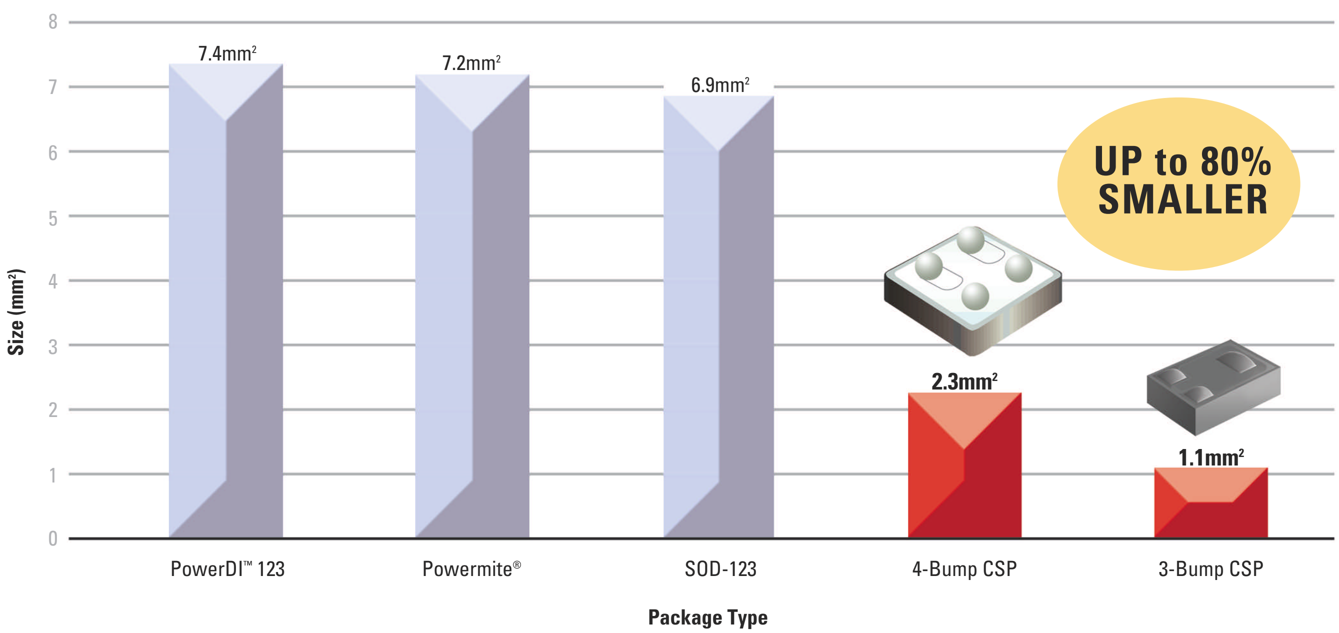

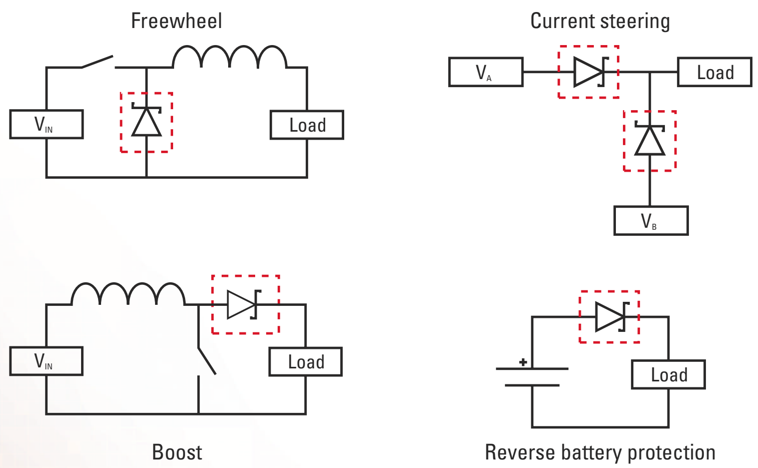

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IR130CSPTR	1.0A	30V	0.33V	100μA	-55 to 150°C
IR140CSPTR	1.0A	40V	0.38V	80μA	-55 to 150°C
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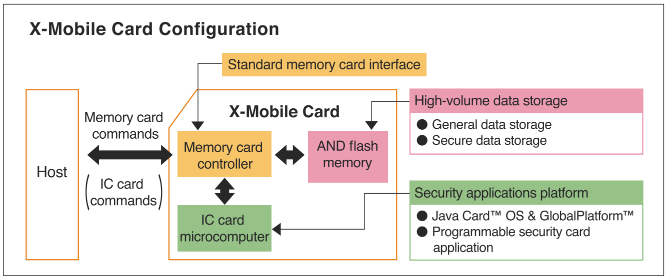

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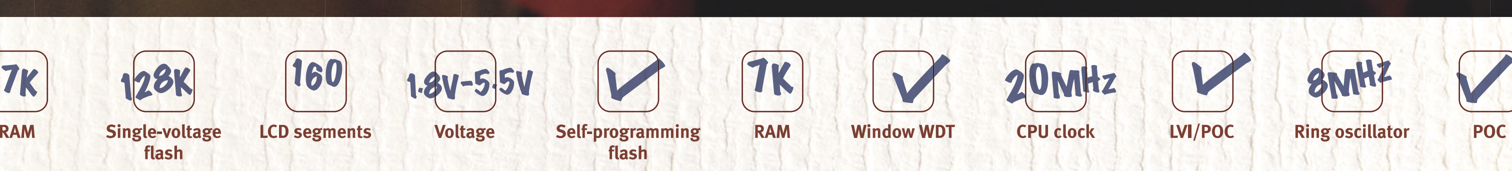

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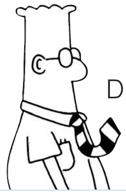

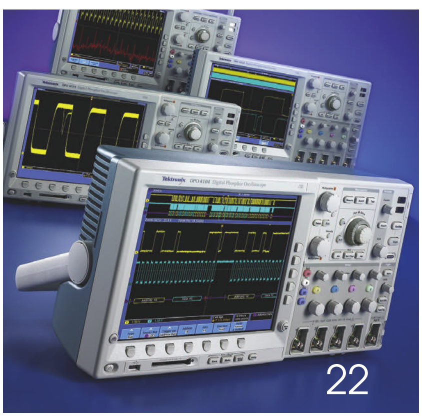
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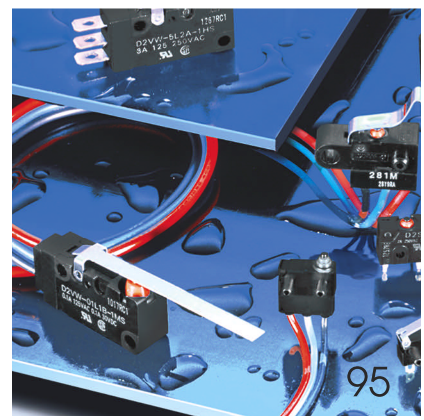
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DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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ADVERTORIAL

A New Approach to Streamlining the Application of Advanced Technologies

Today's increasing silicon complexity drives engineers to continually leverage the latest advances in electronic design. However, no company can afford to have its design teams consuming time and effort adopting individual technologies. Instead, organizations need to focus precious engineering resources where they add the most value—differentiating the company's designs. Additionally, in today's fast-paced markets, missed schedules can mean lost market opportunities. Cadence recognizes that to start designing right away, designers need a proven infrastructure—proven on the types of designs they'll be doing and incorporating the kind of IP they'll be incorporating—with typical application hurdles already flattened. This is the essence of the Cadence Kits approach.

A Cadence Kit is a documented methodology built on a set of platform flows applied to a reference design, which is enabled by standards-based IP and packaged with applicability training. Each kit starts with a reference design—a real design representing a specific vertical market.

The reference design incorporates IP that is integrated and validated with the platform flows. One of the biggest challenges has been the difficulty of using IP in the design process. By building on platform flows and a reference design, Cadence Kits greatly simplify the integration, reuse and enablement of IP.

DELIVERING ON THE KITS APPROACH

The first Cadence Kit focuses on analog/mixed-signal (AMS) because of its pervasiveness across markets, including wireless, wired networking, and personal entertainment electronics. The AMS Methodology Kit minimizes risk by targeting key challenges identified by customers in these markets:

- Fragmented design processes that prevent teams from effectively verifying designs across the analog and digital design domains
- Large quantities of data and long simulations, which hamper modeling, extraction and re-simulation of parasitics
- The challenge of managing multiple power supplies through all stages of design as well as reusing and migrating AMS blocks—both of which demand a predictable methodology

The Cadence AMS Methodology Kit addresses these design challenges by delivering a verified methodology, enabling IP, and applicability training—all demonstrated on an end-to-end mixed-signal design.

The AMS Methodology Kit executes a "meet in the middle" design approach that achieves an optimum balance between the needs for speed and for silicon accuracy. It also establishes a design process that allows teams to work with the analog/mixed-signal content in the context of the complete design—from concept to silicon.

The kit gives designers control of parasitic effects from first-cut route and top-level parasitic extraction evolving to block-level and targeted post-layout re-simulation. It addresses reuse and migration of analog/mixed-signal blocks through a repeatable block creation method. In addition, the AMS Methodology Kit helps teams tackle low-power designs by managing multiple power supplies through a top-down methodology for defining voltage supplies.

For more information on how Cadence Kits enable you to simplify the application of EDA technology for greater design productivity, visit www.cadence.com/kit_info.

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Check out these online-exclusive articles:

Using Mathcad to derive circuit equations and optimize circuit behavior

By James C Bach, Delphi Corp

The general-purpose mathematical-analysis tool provides ample capabilities that engineers can employ in circuit design.
→www.edn.com/article/CA6301377

Tool performs OPC spot fixes on IC layouts

DFM (design-for-manufacturability) start-up Aprio is releasing Halo-Fix, a new tool that allows mask-data-prep engineers and manufacturers to make small LRC (lithography-rule-check) fixes to OPC (optical-proximity-corrected) IC layouts without performing a full OPC run on an entire design layer.
→www.edn.com/article/CA6301290

Embedded agents to monitor, correct VOIP quality

Texas Instruments has announced an embedded-system technology that aims to provide distributed, real-time monitoring—and correction—of QOS (quality-of-service) issues on IP (Internet Protocol)-based services, such as VOIP (voice-over-IP) calls.
→www.edn.com/article/CA6299583

CoWare tool upgrade helps make SystemC models reusable

CoWare has released a new version of its ConvergenSC SystemC simulation environment with new features that allow designers to reuse their SystemC-based transaction-level models.
→www.edn.com/article/CA6301291

Spansion releases NAND-like device for wireless-system market

Spansion Inc is releasing the MirrorBit ORNAND, after a couple of years in development. The device is the company's answer to NAND for the wireless-system market.
→www.edn.com/article/CA6300387

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Help *EDN* honor excellence in electronics engineering. The 16th annual *EDN* Innovation Awards program is now under way. *EDN*'s editors have narrowed down the nominees to a group of finalists, which includes outstanding engineers, products, and technologies in 15 categories and the best contributed articles that appeared in *EDN* in 2005.

Please go to www.edn.com/innovation to get the details on all the finalists and then cast your votes using the online ballot you'll find there.

After we tally your votes, along with votes from our editors and editorial-advisory-board members, we'll announce the winners on April 3 at a gala event in San Jose (see www.edn.com/innovation for details and tickets).

A NOTE ABOUT PDFs

Since 1998, we've been making PDF versions of every magazine article available at www.edn.com, and you've told us that this feature is one of your favorites on our site. We recently changed the way we provide those PDFs. In new articles, simply clicking on "Printer-friendly version / PDF" at the top or bottom of the article takes you to a PDF version that looks just like the magazine page, complete with a toolbar for zooming, downloading, and printing.

FROM THE VAULT

Articles and extras from the EDN *archives that relate to this issue's contents.*

SCOPES: MORE THAN MEETS THE EYE (pg 44):

High-performance DSOs untangle serial-data streams

As electronic systems depend more and more on serial communication, sophisticated digital scopes, powered by clever software, are becoming essential equipment.
→www.edn.com/article/CA608891

Instrumentation amplifier extends DSO

Elusive current waveforms required scope documentation.
→www.edn.com/article/CA6294160

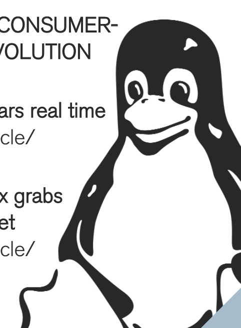
Real-time-DSO bandwidth jumps to 15 GHz

Tektronix has announced what it calls the world's fastest, most-capable, real-time oscilloscopes.
→www.edn.com/article/CA499536

LINUX JOINS THE CONSUMER-ELECTRONICS REVOLUTION (pg 57):

Embedded Linux nears real time
→www.edn.com/article/CA450620

Pick and place: Linux grabs the embedded market
→www.edn.com/article/CA253780



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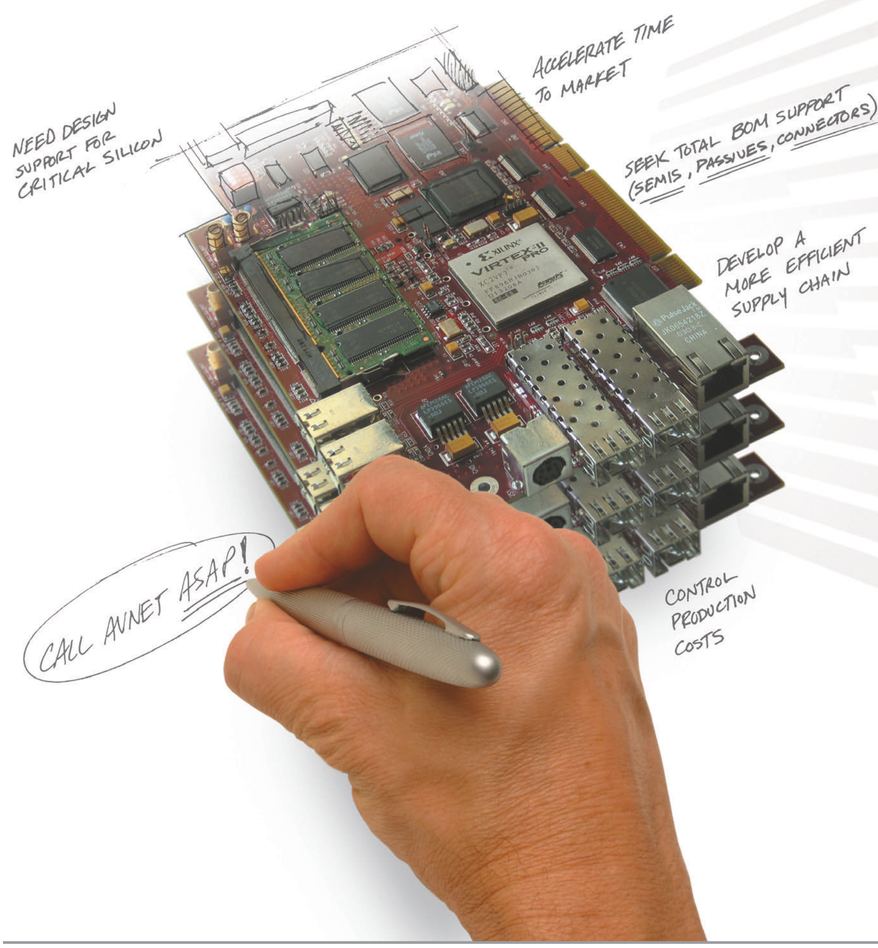

But, partnering with Avnet Electronics Marketing means much more than just having access to the industry's broadest array of design and supply chain services. It means working with a company that is truly focused on exceeding your needs and expectations – a company that is dedicated to giving you **Support Across The Board**.™

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BY RON WILSON, EXECUTIVE EDITOR

From the age of anxiety to the era of the reference design

I suppose introductions are in order. In general, staff changes at a magazine make for poor reading. But now is a time of transition in the engineering profession, so a few changes here may justify taking a moment to say hello—to step out from behind the editorial curtain and chat a bit.

I'm Ron Wilson, and in January, I joined *EDN* as executive editor, working for Editor in Chief Maury Wright. In so many ways, it's a pleasure to be here writing to you today.

As I sit at the keyboard, I'm most of all conscious of a huge pair of unfilled shoes in the office with me. They belong to Bill Schweber, who distinguished this job by his presence over a number of years and through a long list of changes, both great and small. If it weren't for Bill's firm hand, *EDN* would be something less than it is today. I hope I can build on his work and not be the guy who just puts through a couple of ECOs that mess things up.

But enough about me: Introductions need to work both ways. And in a very real sense, the vital part of a magazine is about its readers, not its staff. So who are you?

Therein, as they say, lies a tale. I don't think there has been a time—even in the days when microprocessors were beginning to displace small-scale TTL gates as design tools—when so much has been changing for the engineering community. The changes not only are massive and rapid, but also are happening along a number of axes at once.

Everyone has talked about technology scaling, ubiquitous wireless connectivity, the explosion in software, and the consumerization of the industry. Some have discussed the downsizing of design teams and the slashing of resources. Constant debate continues about the globalization of design—both of work moving out of North America and of the challenges of global design teams. But it's more than that.

A single system can now span so many technologies that it's simply impossible for one design team to understand each of them in detail.

For all of these reasons, we are experiencing a shift in the level of abstraction in design. It's not about a new design language or a new tool set. Rather, we are entering the age of the reference design.

Just as discrete components in many instances gave way to more integrated functional blocks—transistors to op amps, microprocessors to systems on chips—those functional blocks are now giving way to full hardware/software subsystems. Even things that look like components may in fact be whole reference designs in disguise. Is that chip a linear regulator? Or is it a manifold that includes the chip, supporting components, board film, application notes, and test data—all packaged up for the user? Is that video codec a block of silicon intellectual property? Or is it a whole collection that comes with firmware, device drivers, application code, industry certification, a verification suite, and a foundry relationship?

We have encapsulated our components, chips, and boards to hide most of their internal complexity from the designers who must use them. That step has been necessary, because a single system can now span so many technologies that it's simply impossible for one design team to understand each of them in detail. A digital camera may have sensor and display interfaces, image processing, data management, networking, motion control, and system-management functions. So can a machine-tool controller.

So, although we must be specialists in our increasingly narrow area of expertise, we must also have sufficient understanding of a vast array of other technologies to use them as configurable not-so-black boxes. Here is where *EDN* comes in. In the increasing struggle not only to deepen our areas of expertise, but also to broaden our range of effective knowledge, the technology press can be an ally. We hope we can be a powerful one. EDN

Contact me at ronald.wilson@reedbusiness.com.

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To learn more about Ron, visit www.edn.com/060216ed1.

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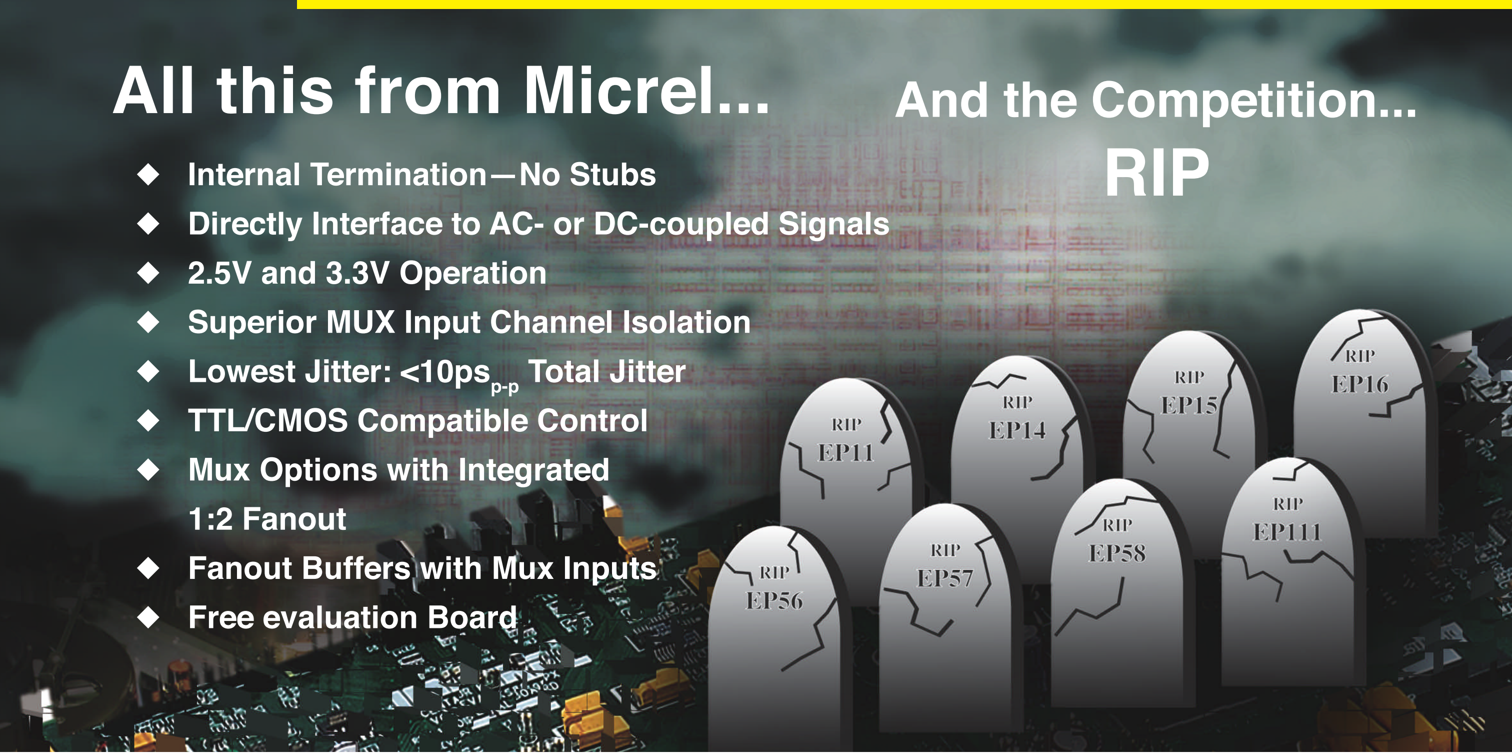

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SY89858U	1:8 Fanout	Yes	5mm x 5mm	$3.79
SY89112U	1:12 Fanout w/ 2:1 Input MUX	Yes	7mm x 7mm	$4.24
		Multiplexers (MUX)		
SY89852U	2:1 MUX	Yes	3mm x 3mm	$2.15
SY89853U	Dual 2:1 MUX	Yes	5mm x 5mm	$3.25
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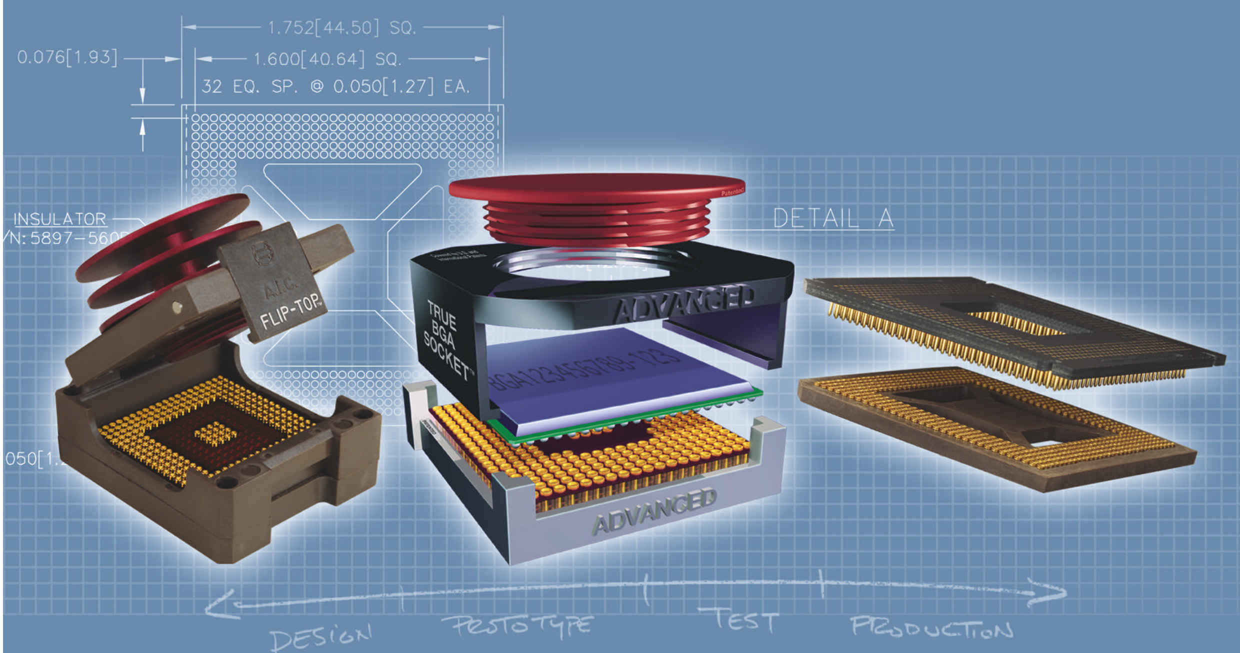

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Vol. IV, Issue 2
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Optimizing Power Management Solutions for Advanced Applications Processors

by Ken Marasco, System Architect

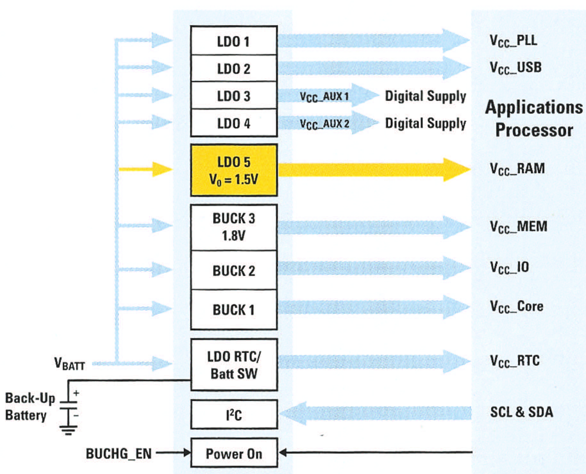


Figure 1. LDO 5 Connected Directly to Main Battery

Power management solutions for today's portable applications processors are becoming highly integrated. Total power consumption, standby, and deep-sleep current consumption effect battery size, bill-of-material cost, and product acceptance. System designers must consider many variations of power supplies when designing portable devices such as smart phones or PDAs. Smart phones are becoming more power hungry and require highly-integrated power management solutions to meet the overall design requirements of maximum battery life in the smallest PCB area possible. Today's applications processors require separate power domains for the core, IOs, memory, and peripherals. The LP3971 is a flexible Power Management Unit (PMU) designed to meet all of these requirements utilizing three high-efficiency buck converters and six LDOs. Applications processors require multiple power-supply voltages, which can be optimized as demanded by the core power manager and system architecture. The LP3971 meets the wide range of system requirements with I²C-controlled output voltages, and factory-configurable power-on sequencing, and default output voltages. This design idea will focus on powering a microprocessor's low voltage rail using the LP3971 buck converter and LDO for a PDA or smart phone application.

When designing a system, the architect must balance an ocean of requirements such as cost, PCB area, component size, talk time, standby time, battery capacity, and schedule. The microprocessor RAM requires a 1.5V supply with a maximum current of 400 mA. Let's start with the simplest, lowest cost solution, a Low Dropout (LDO) regulator connected directly to the Lithium-Ion (Li-Ion) battery as shown in ***Figure 1***. The battery voltage will start at 4.2V and decrease to 3.2V, where the system enters into deep sleep until the battery is recharged or replaced. ***Figure 2*** shows a typical Li-Ion battery discharge cycle.

For the configuration shown in ***Figure 1***, the efficiency of LDO 5 will be:

$$\text{LDO\% Efficiency} = [(V_{OUT} * I_{OUT}) / V_{IN} * (I_{OUT} + I_q)] * 100$$

For this and all other examples in this article, I_q is removed because it is very low (40 µA) compared with I_{OUT} (400 mA).

The efficiency equation then becomes:

$$\text{\% Efficiency} = [(V_{OUT}) / (V_{IN})] * 100$$

For V_{IN} = 4.2V and V_{OUT} = 1.5V, the LDO efficiency is 1.5/4.2 = 36%.

$$\text{Total power } (P_T) = 4.2 * 0.400 = 1.70\text{W}$$

All power that is not delivered to the output load is dissipated as heat within the LDO. Dissipated power is estimated as:

$$\text{Dissipated power } (P_D) = (V_{IN} - V_{OUT}) * I_{OUT} = (4.2 - 1.5) * 0.400 = 1.1\text{W}$$

will be dissipated as heat.

NEXT ISSUE:
Digital Down Conversion

National Semiconductor

Power Management Unit for Advanced Applications Processors

The LP3971 is a multi-function, programmable power management IC, designed especially for advanced applications processors. This device is optimized for low-power handheld applications and provides six low-dropout, low-noise linear regulators, three DC-DC magnetic buck regulators, a backup battery charger, and two GPOs. A high-speed serial interface is included to program individual regulator output voltages as well as on/off control.

Features

- 1.6A Output on three high-efficiency buck regulators with voltage scaling
- Five LDOs for powering peripherals and I/Os with voltage scaling, and a sixth LDO dedicated as a RTC LDO
- I^2C-compatible, high-speed serial interface for software control of regulator functions and settings
- Backup battery charger

The LP3971 is ideal for applications such as PDA and smart phones, personal media players, digital cameras, point-of-sale/barcode scanners, and for powering applications processors such as Intel's Xscale, and other application processors. The LP3971 is offered in a tiny (5 mm x 5 mm) LLP-40 package.

www.national.com/pf/LP/LP3971.html

Dual Step-Down Converter For Portable Systems with Complex Power Management Requirements

The LM3370 is a dual step-down DC-DC converter optimized for powering ultra-low voltage circuits from a single Li-Ion battery and input rail ranging from 2.7V to 5.5V. It provides two outputs with 600 mA load per channel. The output voltage range varies from 1V to 3.3V and can be dynamically controlled using the I^2C-compatible interface. This dynamic voltage scaling function allows processors to achieve maximum performance at the lowest power level. The I^2C-compatible interface can also be used to control auto PFM-PWM/PWM mode selection and other performance enhancing features.

The LM3370 features automatic intelligent switching between PWM low-noise and PFM low-current mode, offering improved system efficiency. And an internal synchronous rectification enhances the converter efficiency without the use of further external devices.

Features

- I^2C-compatible interface
  - V_{OUT1} = 1V to 2V in 50 mV steps
  - V_{OUT2} = 2.3V to 3.3V in 100 mV steps
  - Automatic PFM/PWM mode switching and forced PWM mode for low noise operation
  - Spread spectrum capability using I^2C
- 600 mA load per channel
- 2 MHz PWM fixed switching frequency (typ)
- Internal synchronous rectification for high efficiency
- Internal soft-start
- Power-on-reset function for both outputs
- Operates from a single Li-Ion cell or 3-cell NiMH/NiCd battery and 3.3V/5.5V fixed rails

The LM3370 is ideal for applications such as baseband processors, application processors (i.e. video and audio), I/O power, and FPGA power and CPLD. The LM3370 is offered in a tiny (4 mm x 5 mm x 0.8 mm) LLP-16 package.

www.national.com/pf/LM/LM3370.html

Optimizing Power Management Solutions for Advanced Applications Processors

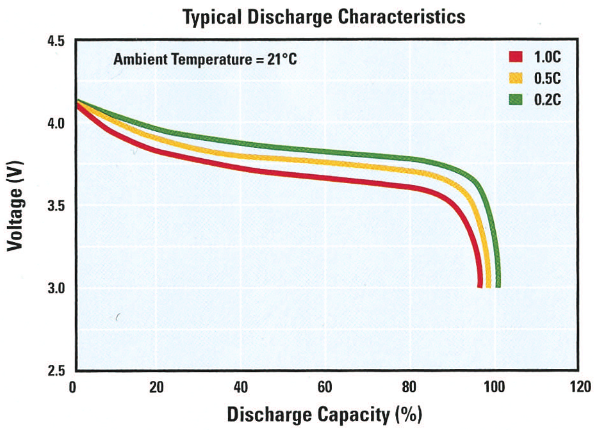


Figure 2. Typical Li-Ion Battery Discharge

We have just calculated the maximum continuous power (P_T). The RAM will not operate at this level for very long. If we look at a 10% duty cycle, the average power consumption will be:

$$P_T = 0.10 * 1.7 = 0.17W$$

The amount of time the RAM operates at I_{MAX} is dependent upon the application, power management firmware, and the operating system.

As shown in ***Figure 2***, the battery voltage does not stay at 4.2V for long. Let's recalculate the power consumption for the nominal battery voltage of 3.6V.

V_{OUT} is still at 1.5V; the LDO efficiency is then 42%.

If the system requires lower power consumption and the configuration shown in ***Figure 1*** is not acceptable, consider the solution shown in ***Figure 3*** where the input of LDO 5 is connected to the output of Buck 3, which is set at 1.8V to power memory.

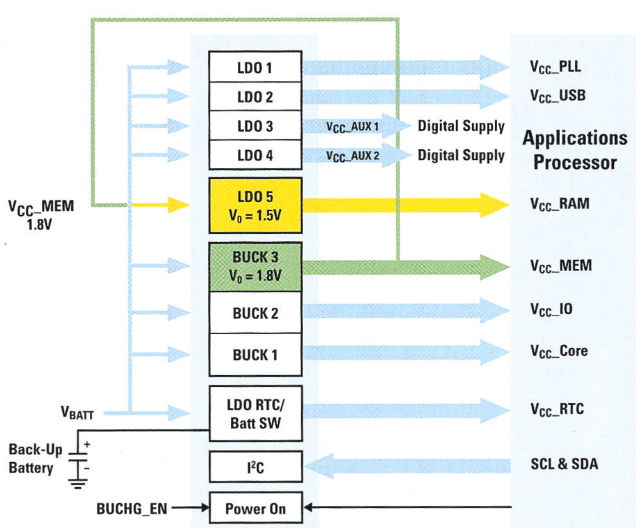


Figure 3. LDO 5 Connected to V_{CC}_MEM

For the configuration shown in ***Figure 3***, when the input of LDO 5 is connected to a 1.8V rail, the efficiency is calculated as:

$$\text{Efficiency} = V_{OUT}/V_{IN} = (1.5V/1.8V) * 100 = 83\%$$

Dissipated power is estimated as:

$$P_D = (V_{IN} - V_{OUT}) * I_{OUT} = (1.8 - 1.5) * 0.400 = 0.12W$$

will be dissipated as heat.

The LDO 5 efficiency is 83%. Yes, it's 83%! Note that if we were to use a switching supply instead of LDO 5, the efficiency could be as low as 85% – an improvement of just 2% for this block.

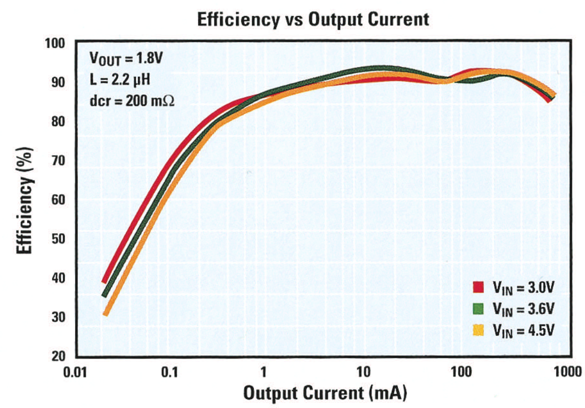


Figure 4. Efficiency at V_{OUT} of 1.8V

However, the overall efficiency depends on the type of converter that is used. Using the efficiency curves from the LP3671 buck converter datasheet (***Figure 4***), the overall system loss due to this double conversion DC-DC + LDO will be 78%. An LDO is the lowest cost, smallest size, and lowest noise solution.

Adding another DC-DC converter to power the RAM will increase the PCB area due to the addition of a very large external inductor (3 x 3 mm) by 10 mm^2 and increase the overall noise of your system. If a 1.8V supply is not available, any buck converter voltage rail that is lower than V_{BATT} can be used. The lower the LDO input voltage, the higher the efficiency—as long as the input voltage is above $V_{OUT} + V_{DROPOUT}$.

Conclusion

There is no reason to worry when using an LDO to power low voltage microprocessors as shown in this article. Ask yourself this question: "Do I really want to use an extra buck converter and inductor to improve system efficiency by just a few percent?" Using a buck converter to power the low voltage rails will increase the size of the PMIC, add another 3 x 3 mm inductor, and increase the BOM cost and PCB area. In contrast, an LDO is inexpensive, small, and easy to use, not to mention the lowest noise solution and it can be optimized for your application. ■

Featured Products

Dual Step-Down DC-DC Converter Features >90% Efficiency Over a Wide Load Range

The LM2717 is composed of two PWM DC-DC buck (step-down) converters. The first converter is used to generate a fixed output voltage of 3.3V, and is available in an adjustable version. The second converter is used to generate an adjustable output voltage. Both converters feature low R_{DSON} (0.16Ω) internal switches for maximum efficiency. Operating frequency can be adjusted anywhere between 300 kHz and 600 kHz, allowing the use of small external components. External soft-start pins for each device enable the user to tailor the soft-start times to a specific application. Each converter may also be shut down independently with its own shutdown pin.

Features

- Fixed 3.3V output buck converter with a 2.2A, 0.16Ω internal switch
- Adjustable buck converter with a 3.2A, 0.16Ω internal switch
- Operating input voltage range of 4V to 20V
- Input undervoltage protection
- 300 kHz to 600 kHz pin-adjustable operating frequency
- Over-temperature protection

The LM2717 is well suited for a variety of applications where multiple high-current, low-voltage power supplies are needed to power system loads, including disk drives, DSP power supplies, DSL and cable modems, TFT-LCD displays, set-top boxes, handheld devices, laptop computers, and other portable applications. The LM2717 is available in a low-profile TSSOP-24 package.

www.national.com/pf/LM/LM2717.html

Miniature, Ultra-Low Noise, 100 mA Linear Regulator for Analog and RF Signal-Path ICs

The LP5900 is a miniature CMOS linear regulator capable of supplying 100 mA output current. Designed to meet the requirements of RF and analog circuits, the LP5900 provides low noise, high PSRR, low quiescent current, and low line transient response. Using a patent-pending design, the LP5900 offers class-leading device noise performance without the use of a bypass capacitor. The device is designed to work with 0.47 µF input and output ceramic capacitors and is available in multiple output voltages from 1.5V to 3.3V, including 1.8V, 2.0V, 2.2V, 2.5V, 2.7V, 2.8V, 3.0V, and 3.3V.

Features

- 6.5 µVrms of noise combined with 85 dB of PSRR ensures signal integrity
- 25 µA of quiescent current extends battery life in portable devices
- 80 mV Dropout improves system efficiency
- ±2% Output voltage accuracy over full line/load/temp
- Thermal-overload and short-circuit protection
- -40°C to +125°C junction temperature range

The LP5900 is ideal for use in cellular phones, PDA handsets, and wireless LAN devices. This linear regulator is available in LLP-6 and micro SMD-4 packaging.

www.national.com/pf/LP/LP5900.html

National Semiconductor

SDR architecture quickly adapts RF-vector-signal generator to changing test needs

When testing devices that conform to multiple wireless standards, fast switching among waveforms is critical for keeping test times within reason. Keithley Instruments' Model 2910 400-MHz to 2.5-GHz RF vector-signal generator incorporates several innovations to reduce test times. Unlike those of competitive instruments, the instrument's outputs settle within 1.5 msec. Moreover, a sync-out, source-settled indicator illuminates only when the source has settled. These features eliminate the need to add wait states to test programs to ensure that the generator's output has settled before the device under test uses the signal. In addition, the instrument's 16-bit-resolution, two-channel, 64M-sample arbitrary-waveform generator supports simultaneous loading of multiple signal waveforms and enables switching among these signals in less than 5 msec.

The unit's SDR (software-defined-radio) architecture adapts as wireless standards evolve. For mobile-phone testing, the unit offers optional built-in signal-generation software personalities for key cellular formats. You can easily upgrade the unit to new and emerging standards as they become available. For signal formats that the initial release does not include, the unit's arbitrary-waveform generator supports downloading of virtually any externally generated signal waveforms with bandwidth as great as 40 MHz. In addition, the instrument can generate RF signals with bandwidth as great as 200 MHz from user-provided analog-baseband in-phase and quadrature signals.

The bandwidth and architecture of the Model 2910 provide a significant future cost savings, because customers need not purchase new RF sources as new wireless applications emerge. The price of the 7-in.-high, half-rack-wide instrument is $14,500. For easy integration into test systems, the generator, which incorporates IEEE 488, USB, and 100 BaseT Ethernet interfaces, conforms to LXI (LAN extensions for instrumentation) Class C. To assist users in quickly developing applications, the instrument includes comprehensive help documentation that is accessible from the front panel, the remote interface, or a CD-ROM.

—by Dan Strassberg

▷**Keithley Instruments**, www.keithley.com.

The Model 2910 400-MHz to 2.5-GHz RF-vector-signal generator incorporates several innovations to reduce test times. The unit's software-defined-radio architecture reduces the likelihood of your having to purchase a new generator to test devices that conform to as-yet-undeveloped standards.

Quad DSP engine features switched-fabric data streams

Curtiss-Wright Controls Embedded Computing recently introduced the Champ-AV6, a VITA (VMEbus International Trade Association) 46 VPX-based DSP engine combining quad PowerPC 8641 devices with serial-switched-fabric communications capabilities. The Freescale (www.freescale.com) 8641 processor has dual integrated 64-bit memory controllers and the Altivec instruction-set extension, which executes as many as eight floating-point operations per cycle. With four 1.33-GHz 8641s, the Champ-AV6 delivers 42 Gflops of peak floating-point performance. Streaming-data-system applications will benefit from the board's 8.5-Gbyte/sec memory bandwidth and as much as 2 Gbytes of DDR SDRAM.

The VPX standard provides backplane connectors that can handle signaling speeds as high as 6.25 Gbps. The board's mezzanine site can accept either standard PMC modules or XMC modules featuring PCI Express with automatic detection of the module type. With PCI Express connectivity, the XMC site provides the high bandwidth to memory for high-performance graphics, networking, and data-acquisition modules.

Software for the Champ-AV6 includes support for operating systems including VxWorks, Linux, and Gedae. Curtiss-Wright provides signal-processing libraries and a high-performance interprocessor-communications library for message passing and bulk data transfers, extending to multiple boards connected through Serial RapidIO. Prices for the Champ-AV6 start at $16,500. Evaluation units will be available in the fourth quarter of this year.**—by Warren Webb**

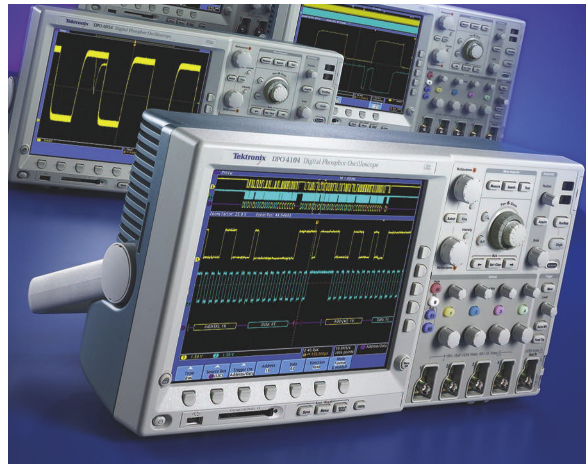
▷**Curtiss-Wright Controls Embedded Computing**, www.cwcembedded.com.

Scopes simplify searching through long waveform records

Tektronix used admirable restraint in not invoking the cliché term "new paradigm" to describe the built-in Wave Inspector tool set of its DPO4000-series 350-MHz- to 1-GHz-bandwidth scopes, which sell for $7000 to $14,000. Tek could legitimately claim that Wave Inspector constitutes a new paradigm for searching through enormous waveform records to find transitory aberrant phenomena. All four of the series members provide waveform memory of 10M samples/channel as a standard feature. In addition, at their −3-dB frequencies, the scopes oversample signals by at least five times. These portable instruments also incorporate lockdown ports similar to those on laptop PCs.

Other notable features include a 10.4-in. color LCD with resolution of 1024×768 pixels—64% more than that of competitive scopes, including units whose displays are equal in size; weight of 11 lb for easy portability; and an enclosure only 5.4 in. deep—shallower, though somewhat wider, than that of Tek's top-selling TDS-3000 series. The units also include front-panel USB and CompactFlash ports and highly evolved triggering capabilities for such serial buses as I^2C, SPI, and CAN (controller-area network).

Wave Inspector comprises a group of zoom, pan, scroll, and search functions in the instruments' hardware and software. These functions enable you to rapidly locate and view rare anomalies in waveform records whose width on these scopes can be as great as 20,000 screens. You access these functions via the front-panel jog/shuttle knobs, two concentric knobs that work together to control zooming and panning. The inner knob controls the zoom factor. The farther clockwise you turn the knob, the more the on-screen waveform view zooms in. The outer ring is a force/rate-sensitive pan control. The more you turn this knob in either direction, the faster the zoom window moves across the waveform.



The DPO4000-series scopes' Wave Inspector controls (upper right of each panel) transform the way you locate anomalous events in records as long as 20,000 screens.

By turning the pan control (the knob's outer ring), you can quickly pan a zoomed window through a long-waveform record. In the resulting pan, the window moves at a speed proportional to the knob's rotation. Pressing the play/pause button causes the window to automatically pan through the entire record. The pan knob controls the speed. This hands-free playback resembles a DVD player's fast-forward control; with it, you can race through a mass of material while watching for visual clues in the waveform. Again pressing the play/pause button immediately stops the panning. A mark function helps you to navigate through the waveform memory. The set/clear-mark button places visible marker symbols on any chosen waveform point. The previous and next buttons instantly move the position in the record between marks, enabling quick cursor placement for timing measurements.

An automated-search feature speeds the search for recurring events or bus-data packets. This innovation most closely resembles a Web browser's search and bookmark constructs. Wave Inspector can search through an entire acquisition and automatically mark every occurrence of a user-specified event, such as a positive-going edge that crosses a voltage threshold.

—by Dan Strassberg

▷**Tektronix Inc**, www.tektronix.com.

FROM THE VAULT

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"During the past year, we talked with many engineers engaged in almost every conceivable phase of the electrical field. 'What, we asked, would you desire most to see in an electrical publication?' The response was as direct as it was unanimous: a magazine of design ideas."

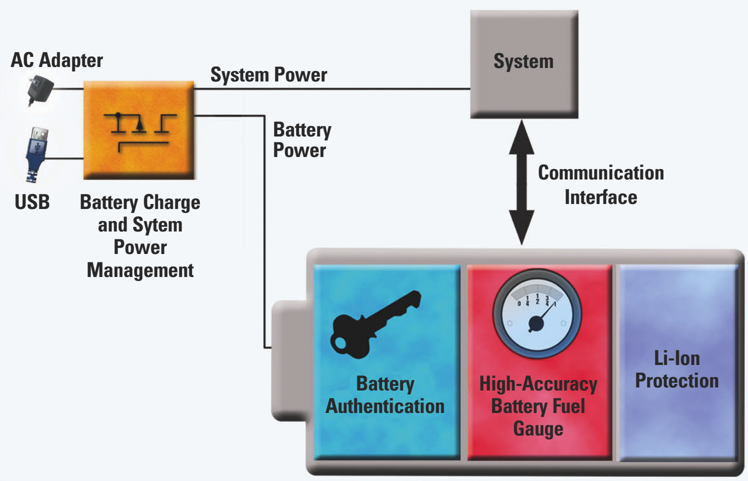
—MS Kiver, Editor, *EDN*, May 8, 1956

DILBERT *By Scott Adams*

POWER MANAGEMENT

Battery Management Solutions for Single-Cell Li-Ion

Power Path Management, Charging, Fuel Gauging and Authentication in Handheld Applications



The **bq24030** charge management device integrates dynamic power path management (DPPM), allowing the AC adapter or USB port to simultaneously power the system and charge the battery.

The **bq27000** fuel gauge provides the system all data needed to effectively manage the battery and extend run-time. It requires no calculations by the host microcontroller, resulting in easy implementation of this accurate fuel gauge.

The **bq26150** identifies batteries or accessories that are approved by consumer electronics manufacturers for full performance of their devices. A simple 5-pin device identifies a battery pack via a single-wire bus using an encrypted response to a host-side challenger.

Evaluation Modules available!

▶ Applications

- Smartphones
- PDAs
- MP3 players
- Digital cameras
- Handheld devices

▶ Features

bq24030

- Power FETs and current sensor, high-accuracy current and voltage regulation, charge status, and charge termination
- Autonomous power source selection (AC adapter or USB)
- AC adapter or USB powers the system directly
- Dynamic charging current based on system requirements

bq27000

- CPU-based IC reports remaining battery capacity, time-to-empty, voltage, current and temperature
- Uses a proven algorithm to adjust calculations for battery characteristics
- Adjusts remaining capacity and run-time prediction for battery inefficiencies

bq26150

- Programmable CRC with a 96-bit unique device ID
- 5-pin, SC-70 package

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Technology for Innovators™ TEXAS INSTRUMENTS

Capacitive isolation moves on-chip

Sporting an isolation rating of 560V operating and 4000V transient, the ISO721 and ISO721M interface devices from Texas Instruments use on-chip capacitors to protect signal lines from becoming pathways to disaster. The result is isolation that is three times faster than optical and 35% faster than inductive, with speeds as high as 150 Mbps. The design also uses less power than optical isolation, is virtually immune to the magnetic fields that plague inductive isolation, and has an estimated MTBF of 25 years.

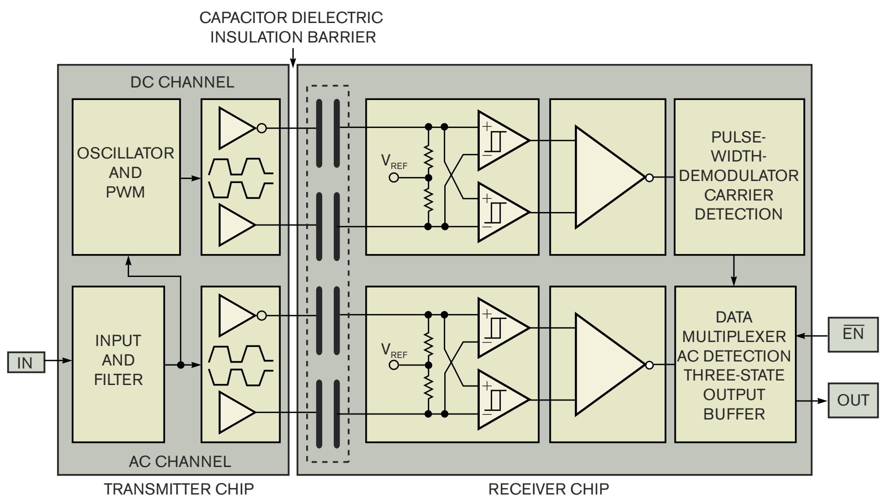
The ISO721 includes built-in noise filtering to eliminate transients shorter than 2 nsec with a 100-Mbps throughput. The ISO721M eliminates the filter to boost throughput to data rates as great as 150 Mbps and reduce latency from 17 to 10 nsec. Both devices have high-voltage transient protection to 25 kV/µsec.

Capacitive coupling normally imposes a highpass-filter response on the signal, but the ISO721 family eliminates that restriction. An input-signal-conditioner stage converts the incoming signal to differential signaling, coupling through on-chip capacitors to a receiver stage. In parallel, a pulse-width-modulation generator senses the low-frequency component of the incoming signal and encodes it before connecting to the receiver stage. The receiver stage recombines both the high- and the low-frequency signal components, replicating the input signal with a 4-µsec delay on the low-frequency component.

The ISO721 multichip modules have two stages of isolation, which take place on separate die; the only connections between them are the bond wires from the first stage to the integrated capacitors that serve as the second stage's input. The capacitive coupling, along with a split lead frame and two-die construction, ensures that no dangerous signals can couple from the input to the output. Devices in the ISO721 family cost $1.65 (1000) and are available now.

—by Richard A Quinnell, Contributing Editor

▷**Texas Instruments**, www.ti.com.



Both ac- and dc-signal components pass through this isolation device, which features on-chip capacitors.

FPGAs get tune-up for high-speed protocols

Altera has added a family of devices for high-speed protocols to its top-of-the line Stratix II FPGA. The Stratix II GX family targets the sweet spot of high-speed protocols, according to David Greenfield, senior director of high-density-FPGA-product marketing. The devices support PCI Express, SDI (serial-digital-interface), XAUI (extended-auxiliary-unit-interface), SONET (synchronous-optical-networking), Gigabit Ethernet, SerialLite II, Serial RapidIO, and CEI-6G-LR/SR (Common Electrical Interface 6-Gbps long-reach/short-reach) protocols. To create the GX devices, Altera replaced the I/O along one edge of a 90-nm Stratix II floorplan with a bank of transceivers. Doing so allows Altera to offer GX devices with as many as 20 transceivers, each operating at 622 Mbps to 6.375 Gbps. A top-of-the-line GX device also has 132,540 logic elements, or roughly 2 million ASIC gates, and 6.7 Mbits of embedded memory.

Each transceiver's receiver channel features a synchronizer, a 8b/10b decoder, a word aligner, a rate matcher, and an equalizer CDR (clock-and-data-recovery) demultiplexer. The transmitter channel offers an 8b/10b encoder and multiplexer pre-emphasis. Clock-management circuitry links the channels. Altera based these choices on the percentage of transceiver customers who are likely to use a block, according to Greenfield. Although 8b/10b encoding and decoding are easy to do in soft or hard logic, Altera puts it into hard IP (intellectual property) because almost every transceiver customer will use it, he says. For XAUI, the company implemented a state machine in hard IP but used soft IP for the standard MAC (media-access-controller) function.

Users furnish Altera with S-parameters, and the company's application engineers use the program to create, in about 45 minutes, optimal settings for equalization and other variables. The GX family will become available for sampling early this year, and volume prices will start at $49 for the EP2SGX30CF780 device.

—by Michael Santarini

▷**Altera Corp**, www.altera.com.

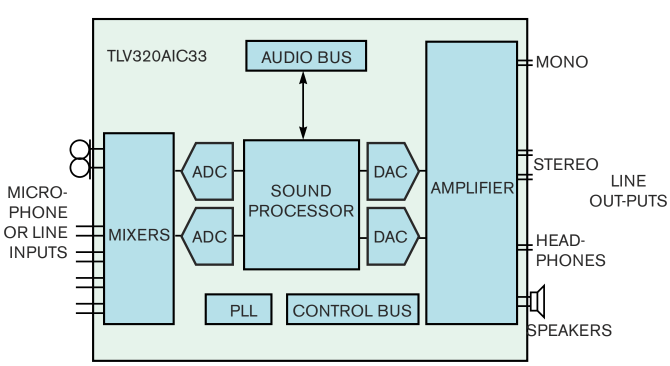
Power-miserly audio codec brings fidelity and 3-D sound to portables

The days of lackluster, tiny sounds from cell phones and other portable consumer products may be over with the introduction of Texas Instruments' low-noise TLV320AIC3x family of 16/20/24/32-bit stereo-audio codecs. With integrated sound processing and consuming as little as 14 mW, the three new devices in the family enable features such as 3-D sound. A demo at the recent CES (Consumer Electronics Show) of the sound of a race car's seemingly zooming around the conference room made for outstanding effects from the demo cell phone's tiny speakers. In addition to cell phones, other applications include battery-powered products, such as cellular handsets, MP3 players with recording functions, and digital still cameras. TI claims that the codecs consume only one-third the power of comparable devices. Their register-based power control enables 48-kHz stereo playback using 14 mW from a 3.3V analog supply.

The TLV320AIC31/32/33 DAC provides an SNR of 100 dB and includes programmable digital filtering for 3-D spatial enhancement; bass, treble, and midrange effects; and speaker equalization and de-emphasis. The devices also provide multiplexing ability among as many as 10 input pins and 10 output pins, as well as fully programmable mixing capability with volume control. A programmable PLL supports the standard audio rates from clocks ranging from 512 kHz to 50 MHz, and it reduces cost and system complexity by eliminating the need for an external crystal. In addition, the TLV-320AIC33 and the TLV320-AIC31 offer differential inputs, which cancel noise that normally enters the ADC.

The AIC31 and 32 are available in 5×5-mm, 32-pin QFN packages, and the AIC33 comes in a 5×5-mm, 80-ball MicroStar Junior BGA package. The AIC31 and AIC32 sell for $3.45 (1000) each, and the AIC33 sells for $3.95 (1000).**—by Margery Conner**

▷**Texas Instruments**, www.ti.com.



Applications for the TLV320AIC3 audio codecs include cellular handsets, MP3 players, and digital still cameras.

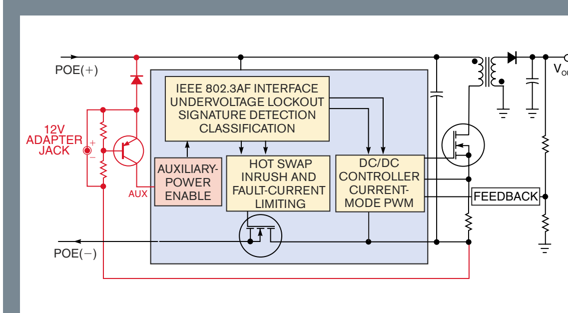
Chip enables POE convenience with auxiliary backup

The potential convenience of POE (power over Ethernet) is undeniable. Users can connect devices such as IP (Internet Protocol) phones, remote cameras, or WiFi (wireless-fidelity) access points with no ac adapter. But designers of POE-enabled products must guard against the possibility that an Ethernet link may not support POE or that users have oversubscribed the power budget of a POE-enabled source. In other words, designers need to prepare for POE power or power from an ac adapter.

Targeting this type of power support, the National Semiconductor LM5071 power IC integrates a PD (POE-powered-device) interface and a current-mode dc/dc-converter controller. An LM5071-based product can operate with ac adapters that output dc voltages of 9.5 to 48V. The dc/dc-converter controller supports various isolated and nonisolated converter topologies, including buck converters. Designers can program functions such as the undervoltage-lockout trip point and hysteresis, as well as adjust the oscillator frequency and duty cycle. Available in lead-free and standard small-footprint TSSOP-16 packages, the IC costs $1.45 (1000).

—by Maury Wright

▶**National Semiconductor**, www.national.com/pf/LM/LM5071.html.



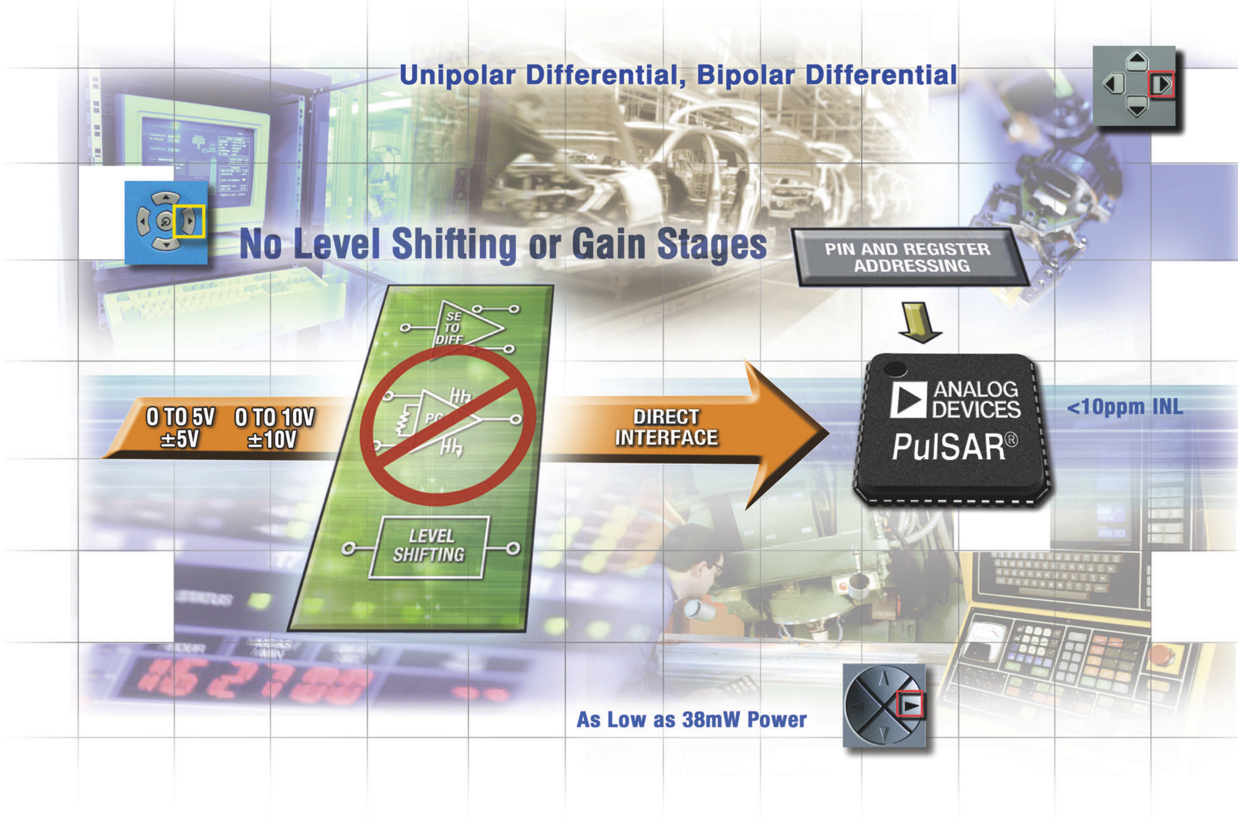
An integrated dc/dc-converter controller and POE interface offer flexibility in connected-product power-supply design.

FEEDBACK LOOP

"Maybe I'll stop blowing up capacitors now. I'll miss the fun, though."

Scott Morgan, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6288037. Add your comments.

18-bit resolution with software-selectable inputs. With SAR ADCs, analog is everywhere.



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AD7612	16	750	85	0 to 5 V, 0 to 10 V, ±5 V, ±10 V	29.45
AD7610	16	250	38	0 to 5 V, 0 to 10 V, 65 V, 610 V	12.90
AD7951	14	1000	100	0 to 5 V, 0 to 10 V, ±5 V, ±10 V	10.99

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ANALOG DEVICES

VOICES

Creating a culture of innovation

Some top executives recently talked with *Electronic News* about how to create and maintain a culture of innovation. These executives included Steve Sanghi, chairman and chief executive officer of Microchip; Rajeev Madhavan, chairman and chief executive officer of Magma Design Automation; Jim Hogan, a veteran venture capitalist in Silicon Valley; and Sanjay Srivastava, president and chief executive officer of Denali Systems. An excerpt of the interview follows. You can find the complete interview at www.reed-electronics.com/electronicnews/article/CA6302393.

What is the secret to creating and maintaining innovation?

A **Madhavan:** When you're a young company, it's easy. You're doing one thing, and the focus is clear. Somewhere in between, when you start working on a product, you lose a little bit of that innovation. For us, we were lucky. One of our competitors got out these big buttons that said 'Got Tape-out.' It was in our face for about six to nine months. It created a culture in the company that we need to take that down.

A **Hogan:** What makes good companies great is that they continue to innovate. There are a lot of companies that have moved out of start-up mode into the time when the initial stock offerings are gone and there are guys coming in from the outside for a variety of reasons. This is where we get into a concept of operational excellence. What distinguishes good companies from truly great companies—and there are not too many that make the leap—are companies that continue to innovate.

When you talk about operational excellence, is this a matter of bean counters keeping tight reins on operating expenses?

A **Hogan:** No, this is bigger. It means that midsized to bigger companies can tolerate no redundancies. In some companies, you'll find five or six competing projects. It's being efficient, making sure everyone's on schedule. But bean counters only see the top line. How you get there is through innovation. Great companies make that leap.

What are the roadblocks to innovation?

A **Srivastava:** Denali is unusual. We started with $10,000, and that is all the investment we have made. We quickly built our first product. We looked at other companies for business

models, and the best we could do was Hewlett-Packard. In the early days of HP, they didn't drive one single product to success. I told our staff that we are starting a project, but I want to reserve the right to kill it because we're starting with unknowns about the market. Part of the culture has been an 80% kill rate. It's not hardware, so our investment is lower. We create a sustainable context for innovation—solving business problems. If you have the entire company behind you, you can create a sustainable context.

A **Madhavan:** We are the opposite. We didn't take $10,000. We took a lot of money because we were funded in the Internet bubble. We had two routing teams and two placement teams. Two teams went at each other. We had some ideas that sounded great on paper and never made it into the product because they weren't going to work. At that time, 50% success rate was our goal. Then, we went to 90%, and now I think we need to cut back to 80%, with 20% being a failure because we attempted to do some new things.

A **Sanghi:** Innovation requires risk-taking. Innovation means going somewhere that you haven't been. If you shoot the person, or shoot the leader, or shoot the team, then you destroy the culture of innovation because no one wants to take the risk. You have to set the culture of the company to 'Why we failed,' instead of, 'Who failed?' In our company, in postmortems, we look at how we came up with wrong information, what didn't we have, and what we missed.

Isn't it the market or the customer that dictates where the innovation should be?

A **Sanghi:** We have application engineers meet in one location three or four times a year. Over the course of several months, they have visited hundreds of customers. In addition to selling the product, they're trying to understand the feature needs of the customer. Many times, the customers don't know what they want. You have to understand the unmet needs of the customers.

A **Madhavan:** In complex design software, there's a bit of a challenge doing that, because, when you go to each customer, each may say that he needs this feature. If you add in all these features, especially with the complexity that chip design is going through, EDA is no longer automated. You're giving tools for this problem or that problem, but you never think about putting it all together.

How important is compensation in driving innovation?

A **Srivastava:** The culture has to reward and value innovation. But modifying behavior with a dollar sign attached to it doesn't work.

–by Ed Sperling, Editor in Chief, *Electronic News*

GLOBAL DESIGNER

Mix measured and simulated circuit data

National Instruments' campaign to broaden the appeal of its LabView product line and to turn it into a single design environment for use at multiple stages in the product-design cycle takes another step forward with the release of Version 9 of the Electronics Workbench EDA Design Suite. NI acquired Electronics Workbench in February 2005. DesignSuite 9 comprises a new release of Version 9 of the Multisim design-capture and -simulation package and the Ultiboard 9 and Ultiroute 9 pc-board-design and -routing software.

Multisim 9 includes a number of upgrades, but the "bigger picture" update is that Version 8 of LabView fully integrates the new software. Users can employ the full range of LabView virtual-instrumentation features and mix real-world measurements with simulation results side by side in the same environment. They can also use real-world data that LabView captures as the stimulus to drive virtual circuits in the simulation environment. Multisim comes with a set of virtual instruments to probe simulated results, but the new release allows users to supplement these instruments with virtual instruments they create in LabView.

In addition to LabView, designers can also transfer data into the SignalExpress package for viewing and analysis: NI says that, because this exchange takes place in the native-file formats of the packages, it eliminates the need for file translation and its potential source of errors.

Version 9 of the package also provides circuit-design assistance with parametric design of op-amp configurations; moreover, you can connect back to the theoretical basis for your circuit design by directly using mathematical language to represent functions in your simulation. As with previous versions of Electronics Workbench, you can download a free demonstration version of the software. Fully functional, the demo version has 50 components, 750 pins, and two pc-board layers. It is, however, a 200-Mbyte download; the company offers a CD alternative. **—by Graham Prophet, *EDN Europe***

▷**National Instruments**, www.ni.com, www.electronicsworkbench.com.

Duo focuses on WiMax

A leader in silicon for fixed IEEE 802.16d WiMax gear, UK-based picoChip has turned to Cambridge Consultants to develop reference designs for the emerging 802.16e mobile-WiMax standard. Many view the mobile flavor of WiMax as potentially more lucrative than the fixed flavor (see "WiMax wireless broadband: Fixed-flavor questions abound, mobile lurks," *EDN*, March 31, 2005, pg 44, www.edn.com/article/CA512128). The technology could become the de facto fourth-generation cellular implementation delivering broadband service to mobile users. Such a service could be a compelling offer everywhere, whereas fixed WiMax may win major business only in regions in which service providers haven't already deployed wider broadband.

The partnership between picoChip and Cambridge Consultants will deliver designs for both the base-station and the client sides of the wireless link. The two claim that the software-centric nature of the implementation will minimize risks associated with deploying a product based on any emerging standard. The plan is for the design to be field-upgradable to meet tweaks in the standard's development. The partners also claim that it will allow designers to add system functions—for instance, moving to MIMO (multiple-input, multiple-output) or smart-antenna technologies. Indeed, picoChip also just signed a partnership with ArrayComm (www.arraycomm.com) to add that company's MIMO technology to picoChip's physical-layer portfolio.

The mobile-WiMax reference designs will rely on picoChip's picoArray silicon. The massively parallel multi-instruction, multiple-data architecture delivers an array of DSP cores to the communication task. The partners are pledging delivery of the reference designs early this year and hope to participate in 802.16e plugfests starting in June.**—by Maury Wright**

▷**picoChip**, www.picochip.com.

▷**Cambridge Consultants**, www.cambridgeconsultants.com.

Configurable-processor technology is now available from Chinese fab house

02.16.06

UK-based ARC International has just partnered with SMIC (Semiconductor Manufacturing International Corp) of Shanghai, China, to bring configurable-processor IP (intellectual property) to SOC (system-on-chip) developers in mainland China. ARC's portfolio includes a range of CPU/DSP cores and multimedia subsystems that can enable compelling digital-media products. SMIC will now offer a one-stop design-and-manufacturing shop for ARC-based designs.

Paul OuYang, vice president of design services at SMIC, says, "As consumer-based products continue to dominate the semiconductor industry, SOC designers seek new ways to reduce their development and manufacturing costs and decrease the time to market for their products. Judging by the increasing interest we are seeing from our customers, we believe that ARC's configurable-processor technology provides one such solution." Semico Research (www.semico.com) states that China's semiconductor industry reached $7.5 billion in 2004. The research company expects SOCs for consumer products to drive future growth.—by Maury Wright

▶**ARC International**, www.arc.com.

▶**SMIC**, www.smics.com.

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Agilent Technologies

BY BONNIE BAKER

Oversampling ADCs: effective versus noise-free bits

If it weren't for the pesky real world, analog circuits would have disappeared long ago. However, entities such as temperature, sound, pressure, and vibration (to name a few) just won't go away. Nevertheless, the trend in the electronics industry continues to drive toward a totally digital system. The industry will never annihilate analog circuits, but with a certain degree of indifference, digital-circuit designers continue to promote their domain of choice.

A digital strategy eliminates many design problems. For instance, the ratio of silicon size to function is shrinking at a much faster rate than that of mature analog systems. Digital-linearization algorithms easily replace complex analog-circuit options. The noise margins of a digital gate are much larger than those of analog and mixed-signal circuits. Of the many challenges that analog designs present to the engineer, noise reduction consumes a large portion of the design time. Analog designers must squeeze the last bit of precision out of circuits by reducing noise.

Because the real world will not go away, the noise that goes along with it is also here to stay. As the digital portion of the system circuit gets closer and closer to the analog front end, it also gets closer to the noise. Engineers that haven't gained respect for this age-old analog issue are usually stunned to find out that the noise in their system at the analog-to-digital interface prevents them from obtaining accurate, repeatable results.

Regardless of architecture, a sampling ADC has noise and distortion sources. These noise and distortion sources can include the capacitor thermal noise in a sampling system, kT/C, where K is Boltzmann's constant, T is temperature in Kelvin, and C is capacitance in farads; resistor noise; aperture jitter; quantization noise; differential nonlinearity; and integral nonlinearity. With the decimation filter and digital interface, this type of ADC's circuitry is almost completely digital.

The general assumption is that the noise from oversampling architectures is gaussian in nature.

When you use an oversampling-ADC architecture, some manufacturers assume that the resulting noise from multiple conversions is random. When you apply a "noiseless" dc signal, such as ground, to the input of the oversampling converter, multiple digital-output codes theoretically generate a gaussian distribution. If the sample is large enough, the standard deviation of the data is repeatable, providing the effective bits for the converter. Given these conditions and assumptions, you can apply an rms or standard-deviation calculation to estimate performance over time as well as provide peak-to-peak or noise-free-bits estimates. The conversion of an rms-bits value to a peak-to-peak-bits value is peak-to-peak bits=rms bits+$\log_2(2\times 3.3)$ bits, where $\log_2(6.6)$ bits=2.723 bits. This formula assumes an industry-standard crest factor of 3.3.

In retrospect, the theory of noise performance of oversampling ADCs has not kept up with actual silicon. Developing the best oversampling converters encompasses using engineering insight, approximations, and theory. The theory behind the noise generation of these types of converters remains underdeveloped. Thus, manufacturers use characterization and test to specify oversampling, converter-generated noise.

The general assumption is that the noise from oversampling architectures is gaussian in nature. You can prove this assumption by looking at several thousands of samples in a histogram graph. You can reduce your sample size to several hundred if you calculate the rms value and then apply the peak-to-peak formula above. EDN

Bonnie Baker is the author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie.bbaker1632@aol.com.*

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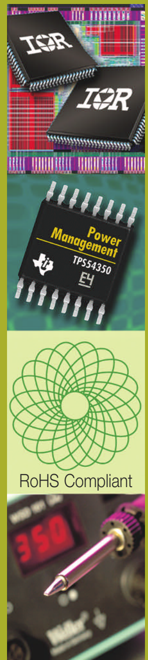

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For expanded analysis and additional internal and external pictures of the PSC805, visit www.edn.com/060216pry.

Sonic surprises

Dissecting the high-resolution hype

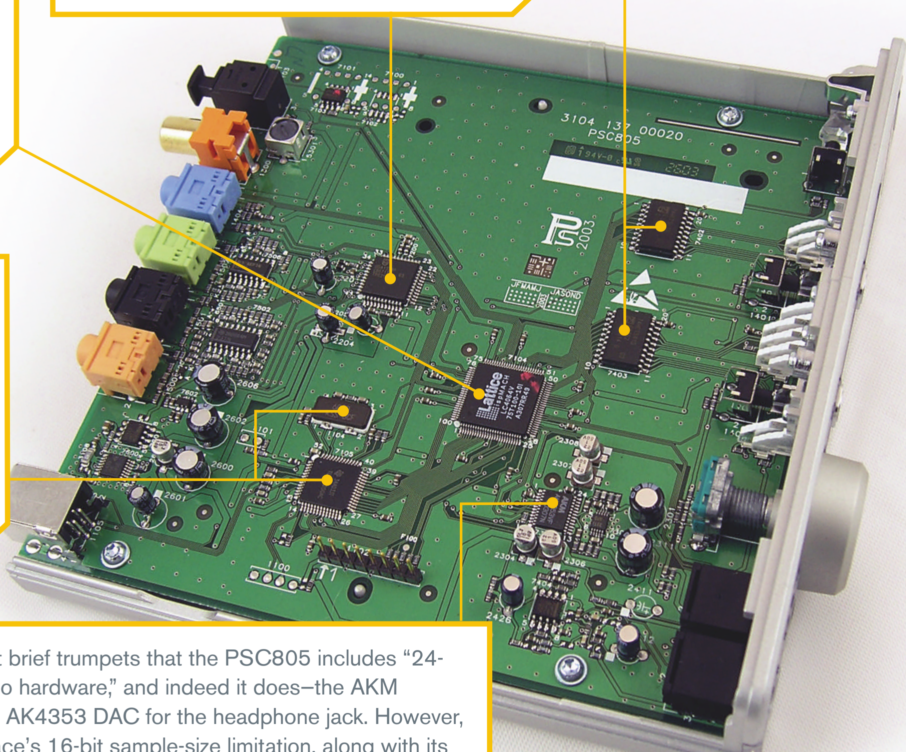
Late August 2005 brought a killer deal from Philips' online store: a PSC805 Aurilium 5.1-channel external sound processor at 60% off its previous $50 asking price. What do $20 plus sales tax and free shipping translate to in terms of included hardware? If you rely on the company's DSP heritage and the product's documentation, it's not what you might think. The PSC805 isn't a bad deal at $20 (or even $50), but don't mate it with an anemic or pre-Windows 2000-powered PC or rely on it to accurately capture your next high-resolution-audio masterpiece.

One big surprise: This high-volume, cost-sensitive consumer-electronics product contains a Lattice Semiconductor 64-macrocell CPLD. Extrapolating from the pc-board traces, it performs a number of gatekeeper functions, such as:

- translating I^{2}C audio to S/PDIF,
- driving front-panel LEDs and generating outgoing commands that route to the PC over USB, and
- responding to incoming commands from the PC over USB and consequently controlling other PSC805 circuitry.

The PSC805 claims to enable you to experience "high-definition 5.1 audio on your laptop or PC." Indeed, the Philips UDA1338H's audio codec's DACs (which work in tandem with amplifiers to drive as many as six speakers) accept 24-bit input sources, and its ADCs output 24-bit I^{2}C-formatted data. But eight of those bits largely go to waste because of the 16-bit-sample-size limitation of the USB connection to the PC, coupled with a reliance on PC-based software for most audio processing.

Another big surprise: The PSC805 also contains discrete logic in the form of two Philips 74HCT541 line-driver ICs that work in tandem with the CPLD to selectively illuminate the front-panel LEDs. The final surprise (or maybe not, given the unit's price tag): no dedicated audio DSP. Instead, bass and treble boost (as well as more general equalization), two-channel audio expansion, six-channel audio virtualization, reverberation, and other audio-processing algorithms run on the host PC.



The unit's packaging touts USB 2.0 support but neglects to include the "full-speed" (12-Mbps) qualifier. The Texas Instruments TUSB3200 streaming-audio controller (with corresponding crystal above it), which the company identifies as a USB 1.1-to-I^{2}C transceiver, reveals the truth behind the marketing propaganda.

Philips' product brief trumpets that the PSC805 includes "24-bit/96-kHz audio hardware," and indeed it does—the AKM Semiconductor AK4353 DAC for the headphone jack. However, the USB interface's 16-bit sample-size limitation, along with its 48-kHz sampling-rate constraint, attenuates the hype.

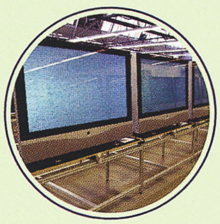
Spend less. Do more. Get there first.

TIME is the driving force: time to knowledge, time to market, time *in* market, and, of course, time to profit.

With today's competitive pressures and short product life cycles, you need to innovate quickly to win in your marketplace. You face an increasing number of competitors, and need to differentiate your product to reach numerous markets. **TIME** is the driving force: time to knowledge, time to market, time *in* market, and, of course, time to profit.

The ideal development solution would allow you to:

- Get your products to market six to nine months earlier than with a standard cell technology flow
- Create your first product at a fraction of the traditional development cost
- Introduce multiple variations of a product—customized to different markets—at the same time
- Move from prototype to low-cost production quickly, while minimizing cost and engineering effort
- Migrate seamlessly to a structured ASIC for a fast path to production (turnaround time in weeks) with up-front non-recurring engineering (NRE) costs at a fraction of ASIC NRE costs



Design Without Compromise

The perfect scenario uses a high-density FPGA as a low-risk prototyping platform that provides the flexibility to test-market your product so you choose the right features before finalizing your design. When you're ready for volume production, you can seamlessly migrate to a structured ASIC that costs up to 90 percent less than the FPGA. And all this is possible with a US$2,000 development software tool.

Altera is the only company that offers this complete prototype-to-production platform to both system and semiconductor companies. With Altera's solution, you can create your designs using existing development tools, including standard EDA tools, then verify the design in-system with an FPGA. You can demonstrate your technology to customers and change your design on the fly, customizing your products for the marketplace and even bringing multiple variations to different markets at the same time. Because you don't have to commit to an NRE cost, risk and investment is minimal, giving you a competitive advantage. And, to protect your designs against

Demonstrate your technology to customers and change your design on the fly, customizing your products for the marketplace…bringing multiple variations to different markets at the same time.

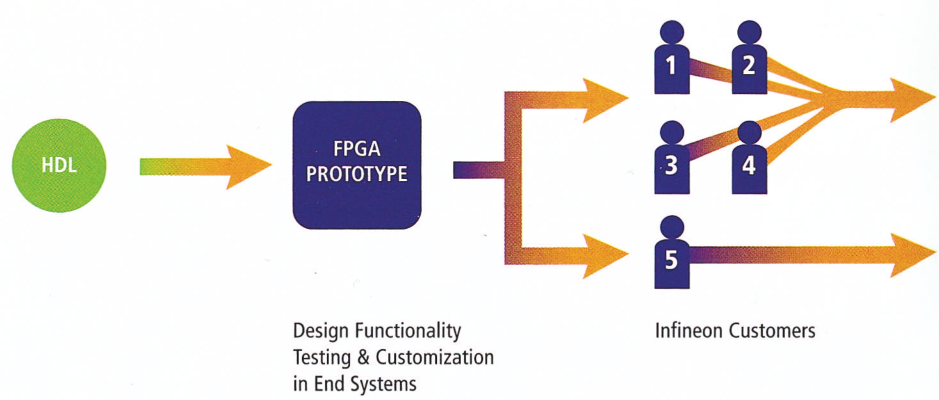
Innovative ASSP Development Model

COMPANY: Infineon Technologies, Communication Group

APPLICATION: MetroMapper 622 ASSP chip, a mapper/framer capable of mapping datacom traffic into SONET/SDH transport payloads

Entering a new market, the Infineon group faced time-to-market pressures, limited engineering resources, limited funding, and multiple customers each looking for customization. Unwilling to risk the time and millions needed for standard cell ASIC development, the Infineon group chose Altera's HardCopy

Infineon Design Flow
Infineon prototyped and tested their design in an FPGA, then created two HardCopy structured ASICs: one was customized for a single customer's requirements, and the other for a broader range of customer needs.



You'll get guaranteed, fully operational structured ASICs in record time, minimizing risk and helping you get to market as quickly as possible.

intellectual property theft, Altera® FPGAs also include built-in, non-volatile encryption.

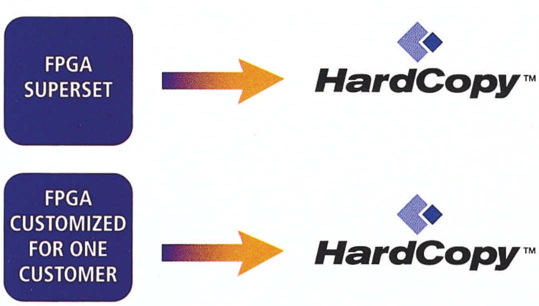
Once the design is finalized, Altera takes over and migrates it to a pin-compatible, functionally equivalent HardCopy® structured ASIC for mid- to high-volume production. There's no need to re-spin the board. You'll get guaranteed, fully operational structured ASICs in record time, minimizing risk and helping you get to market as quickly as possible.

HardCopy Development Flow

The seamless prototype-to-production flow available with Altera's HardCopy devices simplifies design. Engineers simply create and optimize their design for the FPGA and verify the design in-system, then create an archive file to hand off to the Altera HardCopy Design Center. ASIC prototypes are delivered in record time.

structured ASICs. Infineon sent Stratix® FPGA development boards to various customers for design input and created two FPGA supersets, ultimately making a number of customers happy. After in-system validation, the Infineon design was migrated to two HardCopy structured ASICs by Altera.

This unique design methodology allowed the Infineon group to uniquely customize the designs for end customers at a fraction of the cost of ASIC development. The fast turnaround time for HardCopy prototypes enabled Infineon to beat their competition to market.



For more information, visit www.altera.com/hardcopy

Ask the experts.

Get to production in *record* time.

Q How does a structured ASIC differ from a standard cell ASIC?

A With ASICs, all silicon layers are customized. In contrast, structured ASICs start with standard, pre-tested base layers of logic and hard intellectual property (IP), and the proprietary design is then implemented on the top few metal layers. This process saves development time and costs considerably less, but can be risky if you don't verify the design in-system before committing to silicon. Altera offers the only solution with an FPGA front-end, minimizing cost and risk, improving flexibility, and speeding time-to-market.

Q Are HardCopy series structured ASICs pin-compatible with their FPGA counterparts?

A Yes. HardCopy structured ASICs are pin- and footprint-compatible with their FPGA counterparts, eliminating the need to respin the board.

Q How much power reduction can I expect when moving from an FPGA to a HardCopy II structured ASIC?

A HardCopy II structured ASICs can consume less than half the core power of their FPGA counterparts (dynamic and static) because the HardCopy II die is significantly smaller, and because only the logic used in the HardCopy II device is powered on.

Q What design files do I deliver to Altera for the migration process?

A Using Altera's Quartus® II development software, simply generate a Quartus II Archive File (.qar) using the HardCopy Files Wizard. This file contains everything the HardCopy Design Center needs to develop a HardCopy structured ASIC. The Altera HardCopy Design Center manages the migration process.

Q How long does it take to migrate a design to a HardCopy structured ASIC?

A Once all the required design guidelines are met and Altera accepts the design, the design can be migrated to a HardCopy series structured ASIC in two to four weeks. HardCopy prototypes will generally be available within five to seven weeks after you have approved the timing results. Production units will generally be delivered within eight weeks from when the prototypes are approved.

Q Do I need to modify my design or use additional design software to migrate from an FPGA to a HardCopy structured ASIC?

A No. You can use the same Quartus II design software to migrate your FPGA design—including any IP that is part of the design—to a HardCopy structured ASIC.

Q What third-party EDA software can I use to develop the design?

A Altera's design flow supports standard synthesis, verification, timing analysis, and equivalency checking tools from Cadence, Mentor Graphics, Synopsys, and Synplicity in conjunction with Altera's Quartus II design environment, minimizing training time and expenses. The Quartus II software, the only design software that supports parallel FPGA and structured ASIC design and development, also supports the same basic design, register transfer level (RTL) synthesis, place-and-route, and verification flows used by ASIC designers.

For more information, visit www.altera.com/hardcopy

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January 2006.

BY KSHITIZ JAIN, ROHIT JINDAL, BHUVAN MIDDHA, AND ROB SMART • STMICROELECTRONICS

Preview USB performance in an SOC design using a SystemC virtual platform

SYSTEMC TRANSACTION-LEVEL MODELS SUPPORT OPTIMIZATION OF EMBEDDED CODE BEFORE SILICON ARRIVES.

With more software than ever for SOC (system-on-chip) designs, programmers and system architects face a growing and vexing problem: how to evaluate and optimize software performance early in the design phase, well before silicon is in hand. To solve this problem, programmers are turning to virtual platforms, which use software to model the architecture and functions of the target hardware.

When designers carefully perform this task with the help of other software tools, such platforms are proving to be effective ways to make early assessments of important performance measures related to how well embedded software functions and its interaction with yet-to-come hardware. Virtual platforms can predict CPU efficiency, data-transfer and cache-miss rates, interrupt latency, functional hot spots, and other performance measures.

To understand and appreciate the nature and value of virtual platforms, consider the case of one that assesses the performance of a USB system-software stack. The developers' choice is well-justified, given that USB 2.0, with its 480-Mbps transfer rate, makes it a popular choice for carrying real-time audio and video data. As a result, USB is increasingly finding its way into multimedia products, such as set-top boxes and mobile phones.

Such a platform can be especially helpful because USB interactions involve a complex protocol and substantial interdependence between hardware and software. This situation demands that software architects as early as possible not only validate the USB system software, but also estimate the load that the software places on the CPU, as well as the impact of interrupt latencies to ensure that USB is indeed a viable choice.

Such performance predictions require a virtual platform that closely models the functions of actual hardware, including the processor, cache and system memory, USB peripherals, USB EHCI (extended host-controller interface), and USB device. In addition, a profiling tool is necessary to find functional hot spots in the software stack and to accurately predict the time necessary for performing functions. The results the developers obtain with the platform prove to align with theoretical predictions, and the platform proves stable enough to assess the performance of the USB stack on actual hardware. Moreover, the platform accurately reflects changes in performance in cases in which developers modify the software stack.

In this case, designers devised a method of evaluating the per-

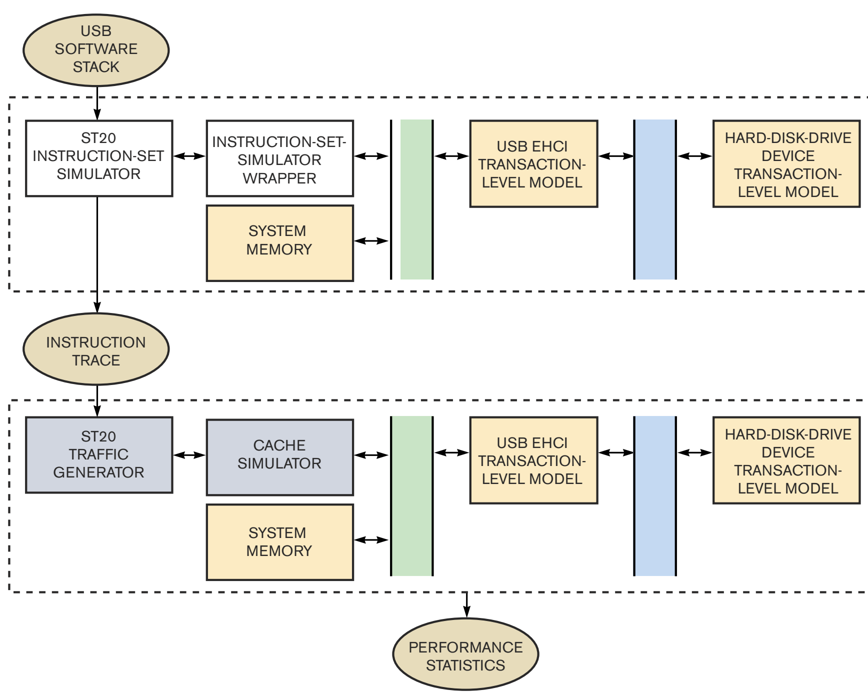

Figure 1 A two-step process first executes the USB software stack on an instruction-set simulator that models the host processor, generating a trace file that records all instruction- and data-memory accesses, as well as any hardware interrupts. In the second step, the trace file passes to a traffic generator that feeds data to the platform's transaction-level models.

formance of the USB system software stack running in a DVR (digital-video-recorder) subsystem embedded within a set-top-box chip. The DVR includes a USB hard-disk drive to record and play video- and audio-data streams. The USB software stack comprises a sample single-threaded DVR application that performs a series of read and write operations with the drive.

The functional platform mimics the operation of the DVR hardware with sufficient detail to reveal important timing parameters. Specifically, the platform models a USB host controller, a hard-disk drive, and system and cache memory. A novel feature of the platform is that it comprises transaction-level models written in SystemC, thus demonstrating this approach as valid for building virtual platforms to evaluate complex embedded software. Developers typically model system-hardware components using RTL (register-transfer-level) models, which represent a lower level of abstraction than the transaction-level models.

PLATFORM SETUP

The virtual platform comprises a USB 2.0 EHCI, a USB hard-disk drive, a cache simulator, a host-processor-instruction-set simulator, and system memory. The USB 2.0 EHCI mimics the functions of the host controller and provides accurate timing values associated with the 480-Mbps data rate, as well as access-memory time, based on a memory model, and write and read times for the EHCI registers. The EHCI also serves as a DMA master, which can make noncached accesses to the system memory.

To trace all instruction and data accesses, the USB software stack runs on an instruction-set simulator, which developers build from transaction-level hardware models. The instruction and data traces pass to the virtual platform, which measures CPU usage, cache-miss rate, and interrupt latency. In addition, Flexperf, a highly configurable, extensible, and modular profiling tool, identifies functional hot spots and helps to debug the software stack.

The system addresses the hard-disk drive as an I/O file divided into sectors and complies with the mass-storage-device specification, including the "bulk-only" specification, from the USB Implementers Forum. As a result, it executes all of the standard device requests accessible through endpoint 0. It also executes a subset of SCSI commands that relate to the DVR through endpoints 1 and 2.

The cache simulator, which models a configurable cache memory, comprises a wrapper around Dinero, an open-source, trace-driven cache simulator. As for the system processor, a wrapper around the instruction-set simulator models a 216-MHz STMicroelectronics C2 CPU core. The simulator converts the processor's memory accesses to transaction-level models. The developers modeled the system memory as a RAM array, and all of the models connect through a transaction-accurate channel roughly based on ARM's AHB (advanced high-performance bus) and a channel that developers modeled loosely on the USB.

Invoking the platform to assess the software-performance parameters involves a two-step process (**Figure 1**). In the first step, the USB software stack runs on the ST20 instruction-set simulator. This action generates a trace file that records all instruction- and data-memory accesses, as well as any interrupts that the hardware initiates. In the second step, a traffic generator parses the trace file and generates equivalent transaction-level operations on a transaction-accurate channel.

The two-step evaluation process represents the normal process of chip design. In the first step, the designer breaks down the design into separate functional blocks operating in parallel to achieve the desired application functions. Therefore, the first platform contains only functional models and no reference time. Using the same functional blocks, designers can have different implementations—mainly timing and performance models—which they perform in Step 2. This approach allows users to try microarchitecture implementations using a common set of reference functions.

The result is a common SystemC-based platform with no external dependencies and with the SystemC simulator's time serving as a reference for evaluating performance. Similarly, the system abstracts instruction and data memory out as SystemC transaction-level models to accurately simulate access times. The two-step approach also makes it easier to link the cache simulator with the traffic generator as a way to model the effect of the cache on the hardware.

PERFORMANCE PARAMETERS

The performance figures that the virtual platform generates derive from the fact that the total time it takes for the SystemC simulator to run the application corresponds to the total time for the application to run on the actual hardware. The application runtime, in turn, depends on instruction-access times as well as latencies associated with the EHCI, cache memories, and other functions. From these values, you can determine key performance measures, such as CPU usage, data-transfer rate, cache-miss rate, and the number of interrupts.

Of these, CPU usage—the percentage of time that the CPU spends executing the software stack—is the most important parameter for evaluating stack performance. It represents time that the CPU is unavailable to run other applications. To determine CPU usage, however, you must first determine and then subtract the CPU-idle time. The idle time is the time that the software stack spends in an idle thread, waiting for a hardware-generated interrupt. This idle time occurs after the sample DVR application commits a block of data to move to or from the hard-disk drive but before the occurrence of the hardware interrupt that initiates the next transfer. You must subtract this time from

TABLE 1 EFFECT OF BLOCK SIZE ON CPU USAGE

Block size (kbytes)	No. of interrupts/iteration	CPU usage (%)
32	Three	40.5
64	Three	27.25
128	Three	17.75
256	Three	13.25
512	Four	11.5
1024	Six	10.75
2048	10	10.25

TABLE 2 EFFECT OF CACHE PARAMETERS ON CPU USAGE

Cache size (kbytes)	Demand misses	Instruction misses	Data misses	CPU usage (%)
1	69,577	52,134	17,443	8.63
2	40,839	32,921	7916	7.72
4	21,911	17,605	4306	7.2
8	11,291	7818	3472	6.86
16	7166	4084	3082	6.82

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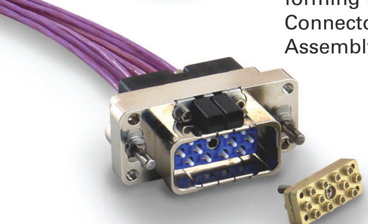

Rugged HD1.25 Terminus and Adapter

the total because, strictly speaking, during that time, the USB software stack does not occupy the CPU.

At this point, you invoke the Flexperf profiling tool to measure the time that the CPU spends in the idle thread. You feed the tool an input-trace file that contains the program counter and the corresponding time, as well as a map file. The map file defines the starting and ending addresses associated with the idle-thread function. From these inputs, the profiling tool calculates the time spent idling, which you then subtract from the CPU time to obtain an accurate figure for CPU usage.

You calculate the data-transfer rate across the USB by dividing the total data moving across the USB, including control, bulk, and protocol information, by the total simulation time to run the sample application. However, USB 2.0's 480-Mbps rate is a theoretical maximum. The actual data rate is much less because of protocol overhead as well as the time spent fetching schedules and data from system memory, especially when the EHCI cache is small. The rate at which software can present that data to the hardware also limits the data rate.

When you provide the Dinero open-source cache simulator with memory-traffic information, it generates statistics on instruction, data, and overall miss rates. From this data, you can determine the best cache configuration. To record the number of interrupts in the ST20 host-processor trace file, you count the number of interrupts that the ST20 wrapper has trapped. These basic performance figures enable you to derive several other parameters, including the total number of executed instructions that the instruction-set simulator reports; the CPU's execution time, which is the total time minus the idle time; the CPU's total instruction-execution time; and the total CPU read and write times.

The performance results you obtain with the virtual platform in this case are mathematical derivations that are beyond the scope of this article. However, the elements of these derivations include the relationships between maximum SCSI buffer size, the amount of data that transfers during a read or a write operation, how long the system software takes to service an interrupt, and the time associated with processing SCSI commands to the hard-disk drive.

Using the virtual platform, you can observe the effects of block size, total data transferred, cache parameters, data-transfer mechanism, stack size, CPU usage, and other key performance data. Significantly, the results using hardware align with the virtual platform's predictions, easily justifying its development. For example, the virtual platform shows that increasing the block size—that is, the amount of data it transfers in each read or write operation—decreases the CPU usage (**Table 1**). The amount of the decrease, however, shrinks for larger blocks. The platform also predicts that CPU usage decreases as the amount of data transferred grows. The platform makes these predictions assuming that the ST20-C2 core runs at 216 MHz; has a 10-nsec cache-hit latency; has a 160-nsec, single-word, memory-access time, and can buffer a maximum of 256 kbytes of data before waiting for a hardware interrupt. The platform also assumes that the cache model comprises 8-kbyte, two-way, set-associative instruction and data caches, each having a 16-byte block. Also, it assumes that the USB transfer rate is 80 Mbytes/sec.

Surprisingly, the platform indicates that cache size has little impact on the performance of the USB stack. One experiment varies key cache parameters of size, associativity, and block size. Although different parameters cause large differences in the demand misses of the total application, the impact on CPU usage is insignificant. In this phase of simulation, you derive CPU usage by subtracting the total CPU time to run the application from the CPU time for initialization, including device enumeration. The results clearly suggest that read and write operations to the hard disk comprise fairly regular accesses to both instruction and data memory. That is, with the read and write operations showing high spatial and temporal locality, the overall number of misses to the hard-disk drive remains nearly constant, regardless of the variations in cache parameters.

Table 2 summarizes the results of varying cache size. Instruction and data caches are the same in all cases, associativity is two, and block size is 16 bytes. **Table 3** shows the results of different associativity values for 8-kbyte caches also having 16-byte blocks. **Table 4** summarizes the results of variations in block size for 8-kbyte caches having an associativity of two. The results assume a 5-nsec cache-hit latency and four-word accesses taking 160 nsec per word.

In contrast to the minimal effects of cache size on CPU efficiency, a wide variation exists between the ways that the EHCI moves data to and from memory. The *copy-semantics* approach moves data from a cached to a noncached region accessible to the EHCI. N*oncopy semantics* assumes that the EHCI can access the memory region containing the desired data. In this approach, the memory region is noncached, and a direct pointer to that location passes to the EHCI.

The widely different performance figures for the two mechanisms occur because with noncopy semantics, no data copies from one memory region to another, eliminating all move instructions and significantly cutting the workload for moving large amounts of data. For example, when transferring 32 Mbytes in 64 iterations of 256 kbytes each, the virtual platform shows

TABLE 3 EFFECT OF CACHE ON CPU USAGE

Cache set-associative count	Demand misses	Instruction misses	Data misses	CPU usage (%)
One	23,173	14,312	8861	7.18
Two	11,291	7818	3472	6.86
Four	8582	5680	2902	6.83
Eight	7331	4501	2830	6.78

TABLE 4 EFFECT OF BLOCK SIZE ON CPU USAGE

Block size (bytes)	Demand misses	Instruction misses	Data misses	CPU usage (%)
4	28,112	17,081	11,031	6.94
8	17,303	11,331	5972	6.92
16	11,291	7818	3476	6.86
32	8978	6406	2572	7.03

TABLE 5 EFFECT OF STACK SIZE ON CPU USAGE

Stack size (kbytes)	Total no. of instructions	CPU usage (%)
15	6,411,704	8.9
64	6,562,020	9.04
167	6,866,921	9.32
269	7,175,012	9.61
371	7,480,699	9.9
474	7,779,426	10.17
576	8,095,716	10.46
679	8,403,217	10.74

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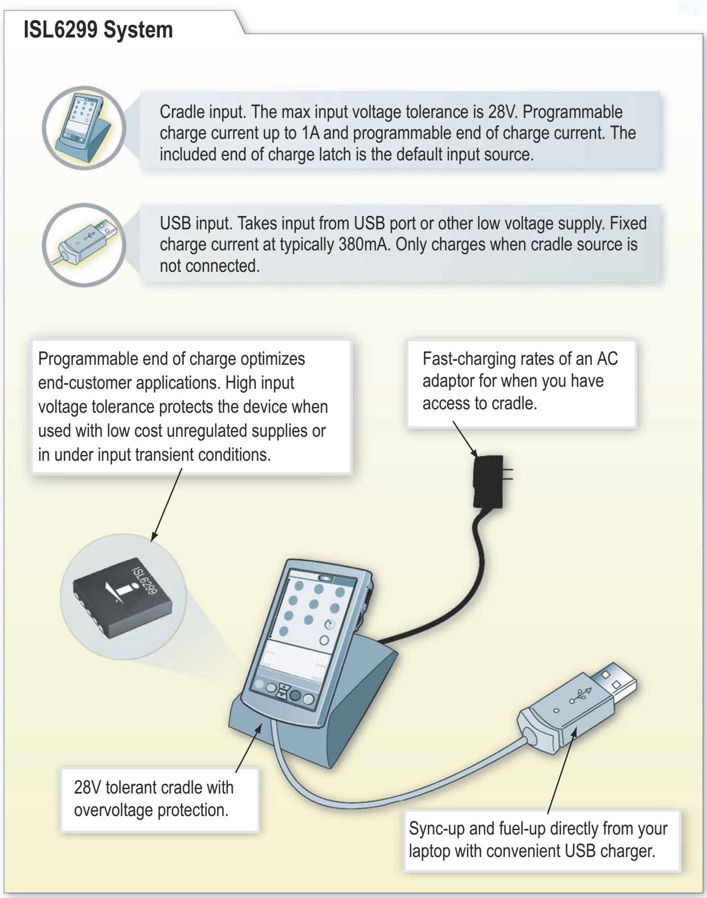

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a data rate and CPU usage, respectively, of 5051 kbytes/sec and 6% for copy semantics versus 7700 kbytes/sec and 40% for noncopy semantics.

In assessing the effect of stack size, the virtual platform yields counterintuitive results in predicting that a smaller stack would cut CPU usage (**Table 5**). Along with CPU usage, the **table** shows that a larger stack also increases the number of instructions executed for an application.

Changing the heap size, however, keeps the results unchanged. (The heap is a region of memory that the software application can directly allocate and deallocate. In contrast, the compiler, rather than the application, manages the stack.) These results, which reflect, as in other cases, a 216-MHz processor-clock rate and a 10-Mbyte/sec data rate, are surprising because the compiler controls the stack, whose size should not matter.

Despite the promising results a virtual platform achieves, it is still in some ways inconsistent with the operation of the hardware. For one thing, the model of the ST20 processor traffic generator is too simple. It assumes that the execution stage for every instruction has a constant average time, which is not always the case. In addition, the traffic generator models neither the processor pipeline nor any pipeline stalls. Nevertheless, some of these factors cancel each other out to give fairly accurate results.

Ongoing efforts are focusing on building more complex platforms and developing seamless methods to evaluate the performance of any software stack. For example, work is under way to combine the virtual platform with profiling tools such as Flexperf, giving software writers and system architects a unified way to evaluate and enhance the performance of embedded code. EDN

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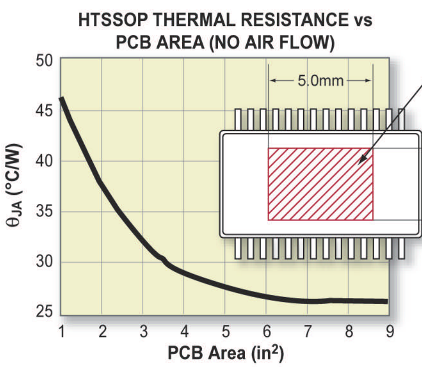

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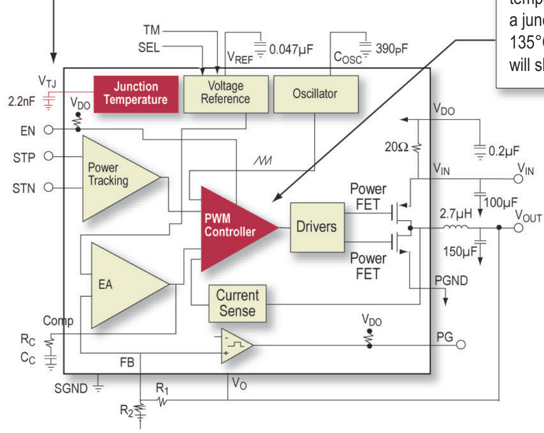

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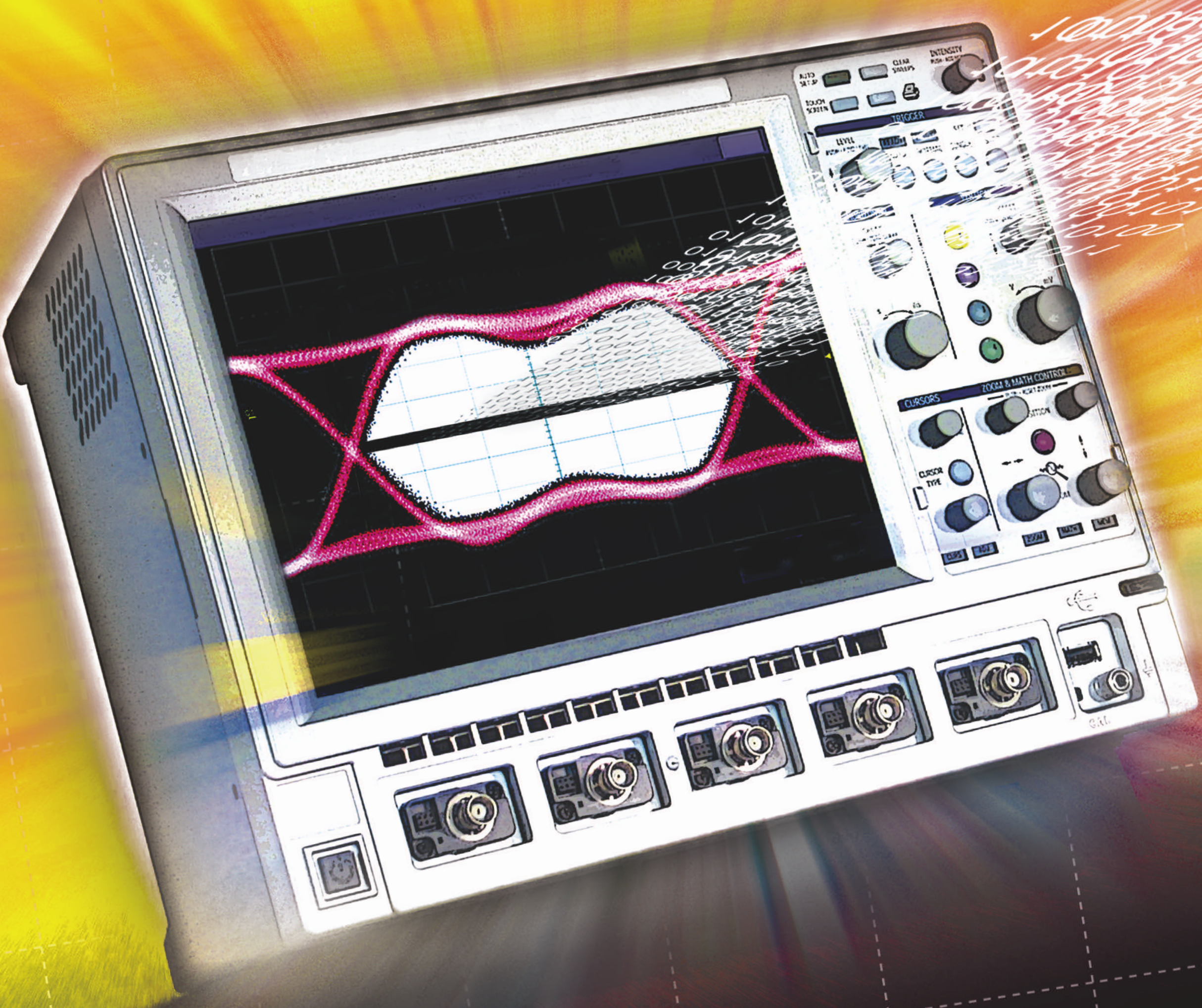
BY DAN STRASSBERG • CONTRIBUTING TECHNICAL EDITOR

SCOPES: more than meets the eye



MODERN DIGITAL SCOPES NOW DO MUCH OF THE HEAVY LIFTING IN MEASUREMENT AND ANALYSIS. BUT SUCCESSFUL USE OF THESE ADVANCED CAPABILITIES REQUIRES DOING YOUR HOMEWORK.

People often say that EEs are almost obscenely fortunate to have a tool that provides as much insight into fundamentally invisible processes as do oscilloscopes into the internal workings of electronic circuits and systems; no other profession has a tool that reveals as much. Despite the embarrassment of riches that scopes afford their users, manufacturers continue to find ways to make the instruments more valuable. Unquestionably, the old cries of "faster" (referring both to bandwidth and sampling rate), "deeper" (referring to depth of acquisition memory), and "less costly" continue to motivate scope designers. But the ways to make scopes even more useful are growing—seemingly just as fast as are bandwidth, sampling rate, and memory depth.

Over the past few years, scopes' analytical and computational prowess has shown no signs of slowing its ascent. Adding analytical capabilities is, however, only part of the challenge of designing computationally intensive oscilloscopes. Another important part is ensuring that new capabilities of mind-boggling sophistication don't actually boggle the minds of the target users. A scope is probably better off without features that are so difficult to operate that users give up trying to make them work. Scope designers often liken their progeny to motor vehicles and refer to the panoply of usability issues under the heading of "How an instrument 'drives.'"

As important as scopes are in EEs' jobs, most engineers still regard the instruments as mere tools—adjuncts to accomplishing the task at hand, *not* the objects of the work. Greater ease of use both responds to and encourages this attitude; when you can make a measurement without giving the technique much thought, it is comforting to believe that the procedure merits little thought. Moreover, in this era of constricted schedules and budgets, there is rarely time to think about problems that seem peripheral to completing a job. Alas, such thinking can be dangerous (see **sidebar**, "Calibrating scopes' high-frequency amplitude accuracy: more difficult than you might think"). Modern scopes make inherently difficult measurements seem easy, but, all too often, the measurements are less straightforward than they appear. Failure to recognize this fact and to understand the instrument and the technique can lead to erroneous or meaningless results—whose lack of validity can go unrecognized until the consequences become painfully obvious and corrective action is prohibitively expensive.

A FOOL'S ERRAND

Becoming enough of a scope expert to select the best unit for your application and to use the instrument in the most advantageous possible way requires effort. Indeed, some say that attempts to find the best scope or to most effectively use it are fools' errands. To begin with, no two engineers are likely to agree on definitions of "best" and "most advantageous" in the context of selecting and using scopes. Second, data sheets, the principal presale documents by which engineers select scopes, have become voluminous, sometimes exceeding 30 pages packed with footnotes and fine print. Third, many midmarket scopes and nearly all high-end units are now PC-based, which usually means based on standard versions of Windows. In such instruments, a Windows-based software application determines how you access the multitude of scope features.

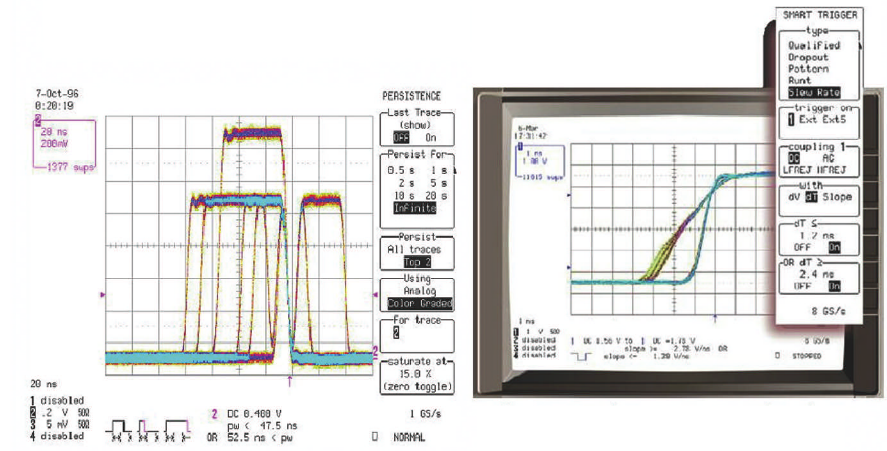
The complexity of scope applications is certainly at least comparable with that of common shrink-wrapped office-software applications, such as Word and Excel from Microsoft (www.microsoft.com). Most office-application users avail themselves of only a small fraction of the software features. So it is with scope users. Moreover, a common problem for many scope users is that they don't use the instruments every day, yet, when they slide into the driver's seat, they need to quickly get answers to their questions about the unit or device under test. In other words, the methods of accessing

AT A GLANCE

- Especially when working with high-speed serial buses, engineers need active differential probes. Scope manufacturers differ on how best to design such probes. Although probing wideband circuits always affects the measured signals, well-designed probes minimize loading effects.

- In response to users' demands to view waveforms in greater detail, some newer scopes sport screens as large as 12.1 in. diagonal.

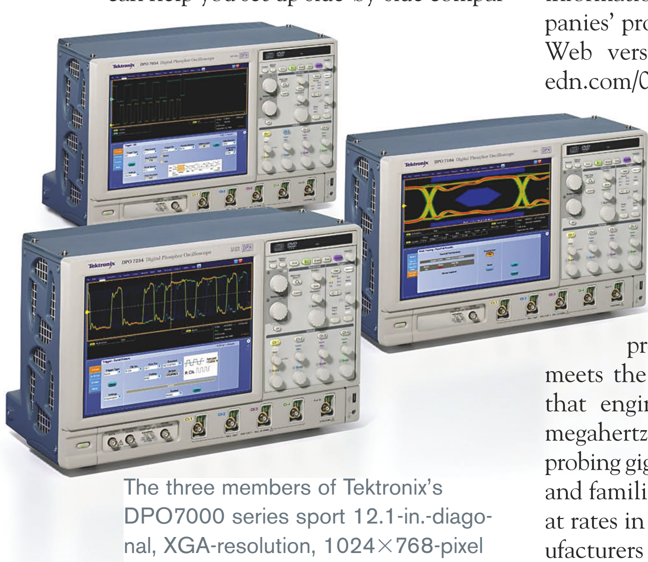
- For the widest-bandwidth measurements, the new NRO (near-real-time oscilloscope) minimizes the drawbacks of sequential-sampling instruments and provides rapid waveform acquisition and deep memory.



Today's scopes can find anomalous waveforms for you if you tell them what to look for. LeCroy calls the feature exclusion triggering. Other manufacturers offer similar features but use different names.

and using scope features should be intuitive—conforming, wherever possible, to the conventions with which the users are familiar.

Scope manufacturers point out that—at least with high-end instruments—your most valuable ally in selecting and effectively using the right instrument can be the field engineer who sold you the scope—or is trying to sell it to you. He can help you set up side-by-side comparisons with competitive units before your purchase and can supply advice and accessories to help you effectively use the scope. Representatives of distributors that sell scopes may offer similar services. Also, don't assume that factory support is unavailable to you because you purchased your instrument from a distributor. Depending on the manufacturer and the scope model you purchased, the factory may offer support. And remember that most scope vendors' Web sites offer a wealth of application notes containing information on effective use of the companies' products. **Tables 1** and **2**, at the Web version of this article at www.edn.com/060216cs, summarize key specifications of real-time-sampling scopes from four major manufacturers.



The three members of Tektronix's DPO7000 series sport 12.1-in.-diagonal, XGA-resolution, 1024×768-pixel screens. The top-of-the-line, 2.5-GHz-bandwidth unit accommodates 400M samples of acquisition memory, all of which you can assign to one channel.

BEGINS WITH PROBE

An appropriate place to begin a discussion of modern scopes is with the probe. The probe tip is where the instrument meets the device under test. Time was that engineers considered only a few megahertz to be a high frequency. Now, probing gigahertz signals is commonplace, and familiar serial buses transmit signals at rates in excess of 3 Gbps. Scope manufacturers recommend that your scope and probe together have a −3-dB bandwidth at least 1.8 times the bit rate. So, if you are working with a bus whose raw bit rate is 3.125 Gbps, your scope and probe should have a combined bandwidth of at least 5.625 GHz. (A bus with a raw bit rate of 3.125 Gbps usually carries information at 2.5 Gbps; 8-bit/10-bit clocking embedded within the data stream limits the information rate to 80% of the raw bit rate.) The bandwidth closest to 5.625 GHz that scope manufacturers advertise is 6 GHz. The 6.67% margin above 5.625 GHz can help to compensate for bandwidth reduction attributable to the probe.

Several points are important. The first is that probing such high-speed serial buses is a job for differential active probes. At these speeds, nearly all buses are differential, and the signal swings are small for a variety of sound reasons: Unlike single-ended circuits, differential receivers tend to reject common-mode "noise," enabling the use of smaller signal swings; differential circuits also radiate less noise and subject power-supply rails to less transient loading than do single-ended circuits. But the smaller signal swings militate against passive probes, which, to reduce capacitive loading, generally attenuate their input signals. In addition, using two scope inputs to view one differential signal is out of the question. That approach effectively not only halves the number of channels on your scope, but also provides input-terminal pairs that are inadequately matched at the frequencies involved. The result can be the appearance on the screen of waveform artifacts that don't exist.

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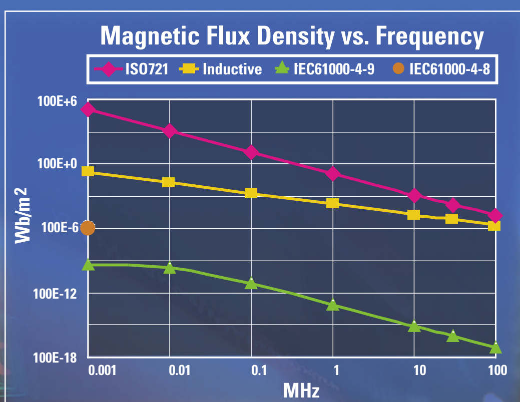

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their sophistication is likely to grow in the next few years. Manufacturers disagree about the best way to design and characterize these devices, but all manufacturers seem to agree on one fact: If you are trying to acquire multigigahertz signals, it is impossible to connect a probe to a unit under test without imposing *some* load on the signal you are trying to measure.

Manufacturers disagree, however, on whether that loading *always* has a *meaningful* effect on the waveforms you wish to view. Nevertheless, it is difficult to refute that, unless a probe is designed with the utmost care, the loading effects not only can be meaningful, but also can make unacceptable waveforms appear perfectly fine or vice versa. For example, probe-induced errors can cause what is, in fact, a good waveform to appear to violate an eye-diagram mask or can make a waveform that violates the mask appear to comply.

That probes impose capacitive loads on units under test is well-known. However, a probe's series inductance is also important in determining the probe's response at several gigahertz. Moreover, the resonance between the probe's shunt capacitance and series inductance can have even more dramatic effects both on the loading of the unit under test and on the probe's frequency and transient response.

PROBES GET SMARTER

Modern probing systems from all of the major scope manufacturers include facilities for bidirectional communication between the scope and the probe. Modern active probes do more than merely send the scope an amplified or buffered replica of the waveform at the probe tips, and the scope does more than just supply power to such probes. For example, LeCroy's newest probes store dynamic

CALIBRATING SCOPES' HIGH-FREQUENCY AMPLITUDE ACCURACY: MORE DIFFICULT THAN YOU MIGHT THINK

By Steve Sekel, LeCroy Corp

Customer questions and complaints about scope amplitude accuracy are fairly common. Customers try to measure the accuracy with a swept sine wave from a signal generator. Users shouldn't try this procedure themselves. Although the measurement sounds legitimate, the results are almost always wrong when the frequencies are higher than a couple of gigahertz.

The first problem is that you need to level the generator output at the output end of the cable. Even the best cables–those that cost more than $1000–have some amplitude loss when you get to the several-gigahertz range. The *only* way to use a signal generator to measure amplitude accuracy is to use a high-quality, calibrated power divider at the end of the cable that connects to the oscilloscope.

One output of the power divider is connected directly to the power head of an RF-power meter that is calibrated for the frequency range and power levels you are testing. If you are testing all of the volts/division ranges, this measurement often requires using more than one power head. The power-meter readings normalize the output level at each frequency step. In an automated-calibration system, you perform this procedure under computer control. It is possible but tedious to manually perform the procedure.

REFLECTIONS

The second problem, which undoubtedly occurs in many cases, is dealing with the reflections from the scope input. In reality, the user is measuring the signal with the reflections superimposed. Scope inputs are not perfect 50Ω terminations. Different attenuators switch using relays or electronic switching. Inevitably, the paths are imperfect; they introduce some reflections at different frequencies.

Scope vendors work to minimize these reflections, but they all achieve about the same performance: a VSWR (voltage-standing-wave ratio) that, over the passband, can go from a perfect 1-to-1 to about 1.35-to-1. Whenever the termination reflects energy back into the line, the reflection creates standing waves at some frequency that relates to the length of the cable. Because they exhibit reflections at different frequencies, different models of oscilloscopes measure different amplitudes from the same generator-and-cable combination.

A user can reduce this effect by installing a high-quality, 6-dB attenuator at the scope's input and attaching the power-divider output to the attenuator. The attenuator improves the return loss by 6 dB, reducing the effect of the reflection in the cable.

As you can see, the metrology required to accurately measure a scope's amplitude accuracy over frequency is complex. All scope manufacturers put considerable effort into designing and verifying the complex systems that designers use to calibrate the instruments. Attempting to manually replicate this measurement by using only a signal generator and cable can't produce results of the desired accuracy.

AUTHOR'S BIOGRAPHY

Steve Sekel is a product-marketing manager at LeCroy Corp. He has worked in the test-instrumentation industry for 28 years, serving in marketing, product-development management, and design engineering. He has a bachelor's degree in electrical engineering from Tri-State University (Angola, IN).

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- 280 MHz, -3 dB bandwidth (A_V = +2, V_{OUT} = 2 $V_{P\text{-}P}$)
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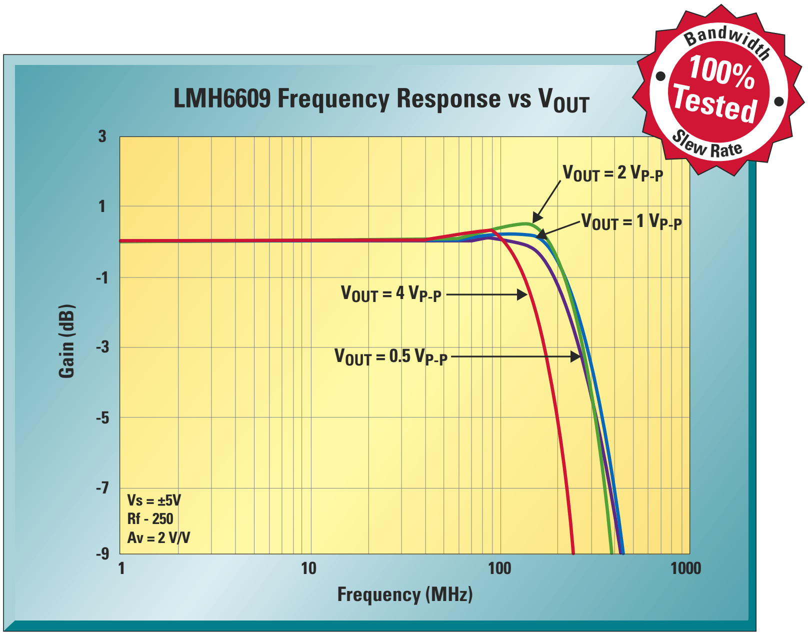

Additional LMH High-Speed Amplifiers

Device	Description	Features
LMH6645/46/47	Single/dual/single with shut-down, RRIO amplifiers	55 MHz Small signal bandwidth, 0.73 mA/ch supply current, 2.5 to 12V supply voltage, 22 V/µs slew rate
LMH6654/55	Single/dual, low-noise, low-distortion amplifiers	250 MHz Small signal bandwidth, 2nd/3rd HD: -80/-85 at 5MHz, 4.5 nV$\sqrt{Hz}$ voltage noise, 1.7 pA$\sqrt{Hz}$ current noise, 4.5 mA/channel supply current
LMH6657/58	Single/dual, high-output current amplifiers	270 MHz Small signal bandwidth, 700 V/µs slew rate, CMIR < 0V, 3 to 12V supply voltage, 110 mA output current
LMH6682/83	Dual/triple, low-power video amplifiers	190 MHz Small signal bandwidth, 940 V/µs slew rate, CMIR < 0V, 3 to 12V supply voltage

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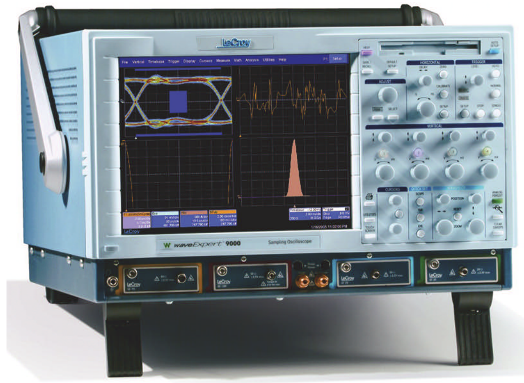
probe-calibration data. This data includes more than just the probe's offset voltage and dc gain; it includes high-frequency-gain- and phase (delay)-characterization data. According to Mike Lauterbach, PhD, LeCroy's director of product management, all ultrawideband scopes from all manufacturers use DSP-based techniques to correct the vertical-amplifier high-frequency-gain and -phase characteristics. The corrections improve the response so that it more closely resembles the desired response—often that of a fourth-order Bessel lowpass filter—than does the amplifier's uncorrected response.

As far as Lauterbach knows, however, only LeCroy's WaveLink probe family currently includes the probe response in the correction algorithm. Within seconds of your connecting a WaveLink probe to a compatible LeCroy scope, the correction routine uploads the calibration data from the probe and compensates the channel's vertical response for the probe's ac characteristics (as measured at the factory—or the last time you used a LeCroy-supplied fixture to characterize the probe). Including the probe in the calibration enables LeCroy, whose 11-GHz scopes offer narrower −3-dB bandwidth than that of the nearest competitive models from Agilent or Tektronix, to nevertheless claim the most accurate high-frequency ac and transient response among real-time scopes in the more-than-10-GHz class. LeCroy also points out that, unlike at least one competitor, it does not currently use DSP to extend the bandwidth of its scopes.

In case you haven't noticed, modern wideband scopes do not have frequency response related to the 10 to 90% rise time by the time-honored formula $T_R=0.35/BW$, where T_R=10 to 90% rise time and BW=−3-dB bandwidth. And you can't determine the combined rise time of the scope and probe from $\sqrt{(T_{R(SCOPE)}^2+T_{R(PROBE)}^2)}$. For one thing, you must carefully check the data sheet's notes to determine whether each rise-time spec applies to the time the signal takes to traverse 10 to 90% or 20 to 80% of the input-step amplitude. Manufacturers sometimes specify both rise times.



LeCroy's WaveExpert, NRO (near-real-time oscilloscope), and SDA100G sampling scopes form a series that you can equip with sampling heads that provide 100-GHz bandwidth on four channels. Although they don't sample in real time, they sample 50 times as fast and store records many times as long as those of sequential-sampling scopes, the only scopes whose bandwidth is nearly as wide.

Some standards for bus physical layers use only the 20 to 80% values; using 10 to 90% values in such cases would only cause confusion. In addition to the "which-rise-time?" issue, however, the old formulas don't apply to new scopes and probes because the newer units' high-frequency-roll-off characteristics differ from those of the analog scopes whose behavior formed the basis for the old rules. To learn more about deep memory and finding ephemeral anomalies in long-waveform records, see **sidebar** "Acquisition memory: a deep subject" at the Web version of this article at www.edn.com/060216cs.

IT TAKES PERSISTENCE

Persistence mode doesn't work quite the way many people think it does (**Figure 1**, pg 52). To dispel the confusion, here is a brief explanation that generally applies to all scope brands. Note that persistence mode can often correctly acquire waveforms that—because of a limited real-time sampling rate—contain frequencies too high for the scope to capture in real time. Many scope users erroneously believe that capturing such waveforms requires using random equivalent-time sampling, a mode you must use with caution to avoid little-understood pitfalls (**Reference 1**).

To use persistence mode, the trigger must be stable in time with respect to the waveform that you want to capture. You can trigger on a waveform feature or use another trigger source. Each time it triggers, the scope acquires waveform samples and places the corresponding dots on the screen with respect to the trigger time. It draws no line between the dots, though. By default, some scopes add sine x/x-interpolated dots, whereas others add none. The scope simply places the dots on the screen—or, to be more exact, it places the dots in an array in the display-processor IC, which draws the dots on the screen. The scope draws no line through the dots, however, and makes no attempt to re-create the shape of the incoming signal; such an attempt could violate the Nyquist criterion.

The scope then triggers repeatedly. Typically, it triggers several hundreds—or even thousands—of times. Each time, it acquires samples and places the dots on the screen, but it never attempts to "draw the trace." The scope simply displays the acquired samples with respect to the trigger time. If the trigger and the incoming waveform are stable, the set of dots is closely packed onto a line shaped like the signal and strongly resembling a waveform. If the trigger time or the waveform is unstable because of vertical noise or timing jitter, the persistence display shows a cloudier set of dots. If the signal shape exhibits occasional large, intermittent aberrations, you may see a large number of dots that follow the normal signal shape and a fainter number that show the abnormal shape.

SLOW REFRESH

Scope manufacturers make much of their instruments' fast screen-update rates and responsiveness to changes in control settings. Some companies refer to such attributes as "analog-scope feel." These claims are valid as well as important to the way in which you use a scope, but, if you think about the claims for a few moments, you can easily wonder how they can possibly not be exaggerations. Nearly all digital scopes refresh their screens only 30 or 60 times per second, yet many display many thousands of waveforms per second. They achieve this responsiveness by aggregating multiple changes to their screen bit maps between refreshes and displaying the

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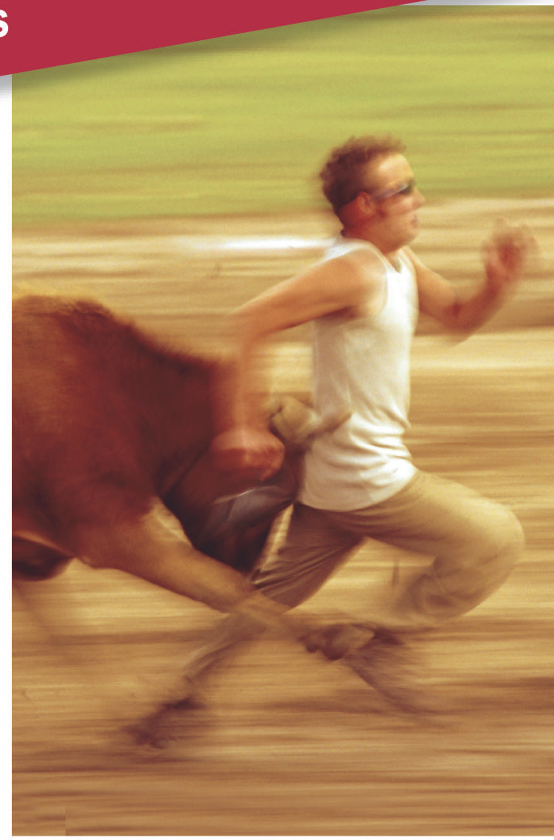

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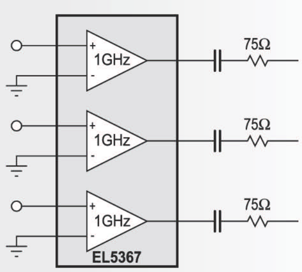
- 8.5mA per channel supply current



Part No.	BW (MHz)	SR (V/µs)	IS (mA)	AV (min) (V)	IOUT (mA)	VOUT (V)
EL5360	200	1700	0.75	1	70	±3.4
EL5362	500	2500	1.5	1	100	±3.6
EL5364	600	4200	3.5	1	140	±3.8
EL5367	1000	6000	8.5	1	160	±3.8

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- Less than 9mA power consumption

Part No.	# of Amps	BW (MHz)	SR (V/µs)	IS (mA)	AV (min) (V)	IOUT (mA)	VOUT (V)	VOS (max) (V)
EL5160/1	1	200	1700	0.75	1	70	±3.4	5
EL5162/3	1	500	4000	1.5	1	100	±3.6	5
EL5164/5	1	600	4700	3.5	1	140	±3.8	3.5
EL5166/7	1	1400	6000	8.5	1	160	±3.8	5
EL5260/1	2	200	2000	0.75	1	70	±3.4	5
EL5262/3	2	500	2500	1.5	1	100	±3.6	5
EL5462	4	500	2500	1.5	1	100	±3.6	5

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- Almost zero overshoot
- Low power consumption

Part No.	# of Amps	BW (MHz)	SR (V/µs)	VN (nV/√Hz)	IS (mA)	IOUT (mA)	VOUT (V)	VOS (max) (V)
EL5100/1	1	300	2200	10	2.6	100	±3.4	5
EL5102/3	1	400	2200	6	5.2	150	±3.7	5
EL5104/5	1	700	4500	14	9.5	160	±3.8	5
EL5202/3	2	400	2200	6	5.2	150	±3.9	5
EL5204/5	2	700	3000	10	9.5	160	±3.8	10
EL5300	3	200	2200	10	2.5	100	±3.4	4
EL5302	3	400	2200	6	5.2	150	±3.7	5
EL5304	3	700	3000	10	9.5	160	±3.8	10

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aggregated result at the next refresh.

This aspect of scope operation is philosophically similar to the way in which scopes whose displays have, say, 1024 pixels horizontally display million-point-deep records without forcing you to scroll endlessly through the long records. However, you can zoom to that mode, as well, if you choose. The simplest way to compress a million samples into 1000 pixel columns, each representing 1000 samples, is to find the minimum and maximum signal values in each 1000-sample group and illuminate all pixels in the column from the one that corresponds to the lowest value to the one that corresponds to the highest. This approach produces a "fat" trace, whose illumination is constant over its width. To show greater signal detail, a scope can determine how many times since the last screen update the signal level corresponded to each point in the screen's pixel map and relate each pixel's brightness or color to the number of "hits" at the associated point.

Scope manufacturers are also discovering the value of the big screen—not the living-room-dominating size of an HDTV and not even the wide aspect ratio of the screens on some laptop PCs but considerably larger in area than has been customary in scopes. Bigger screens on scopes make it easier to see waveform details. LeCroy started the trend a couple of years ago—at least in small-footprint scopes—with its WaveSurfer family, whose members sport 10.4-in.-diagonal, SVGA, 800×600-pixel screens in a 6-in.-deep package that occupies no more benchtop area than does a Tektronix TDS3000B, whose screen measures only 6.4-in. The WaveSurfer's screen area is more than 2.5 times as great as that of the Tek unit. Now, LeCroy has added higher performance units to its stable of large-screen, small-footprint scopes. The three members of the WaveRunner Xi series, whose prices start at $7500, are the same size as the WaveSurfers and also have 10.4-in. SVGA screens.

Not to be outdone, Tek, with its new DPO7000 series, has one-upped LeCroy on screen size and resolution. The DPO-7000 screens measure 12.1 in. diagonal. Their area is approximately 3.6 times that of a 6.4-in screen, and they provide XGA, 1024×768-pixel resolution. The approximately 12-in. package depth is roughly twice as great as that of LeCroy's small-package units but is much shallower than most scopes. The DPO7000s, whose top-of-the-line unit can accommodate memory as deep as 400M samples—all of which is assignable to one channel—also attack LeCroy's long-held dominance in memory depth.

Although welcoming the large screens and small benchtop footprints, engineers who incorporate scopes into larger systems—for example, for production test—may be less than thrilled with the new package geometries. For these engineers, selecting system components that occupy a minimum of rack space is of key importance. The new packages are taller than those of most traditional scopes. It seems likely that the solution to the height problem will lie in LXI (LAN extensions for instrumentation), a new standard for system-component instruments. You can imagine low-profile LXI scopes whose screens lie flat atop them until an operator pulls them forward on their rack slides and hinges the screen into a vertical position.

BEYOND 20 GHz

A survey of the current state of digital-scope technology would be incomplete without some discussion of the widest bandwidth scopes—the class of instruments that engineers used to call sequential-sampling scopes. Until the advent, a year ago, of LeCroy's WaveExpert and SDA100G series, the phrase "sequential sampling" was appropriate, and there were only two vendors, Agilent and Tektronix.

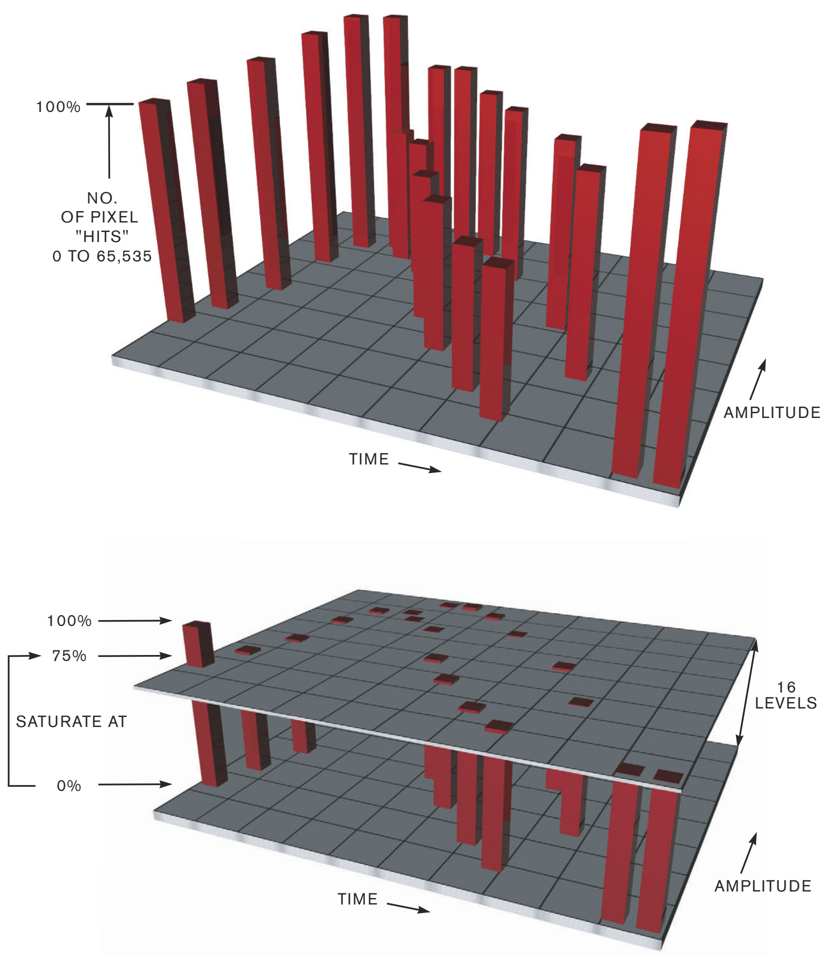

Figure 1 Analog-persistence mode maps frequency of occurrence into intensity or color variations on each pixel of the display simulating the phosphor response of an analog oscilloscope (courtesy LeCroy).

Intersil Video Products

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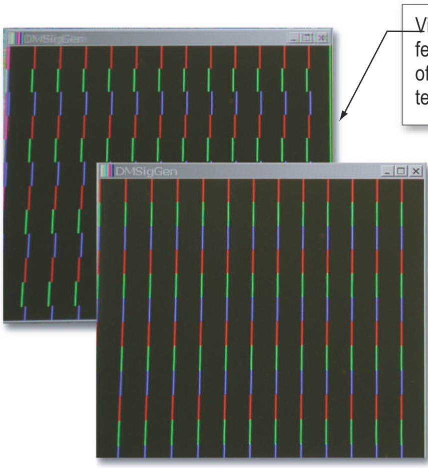
Video Performance Over CAT-5 Cable Driving You Crazy?

Intersil's EL9115, a triple analog delay line, compensates skew introduced by CAT-5 cable, enabling high-quality video through 1,000 feet of cheap twisted pair cable.

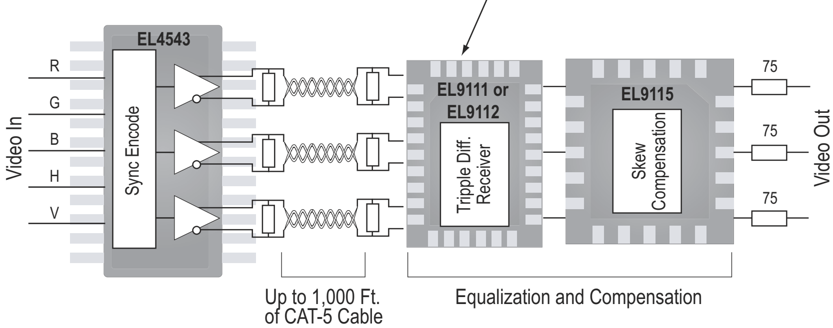
The EL9115 allows three channels to be independently delayed in 2ns steps, up to 62ns. This allows de-skewing of signals, such as RGB video that is transmitted over CAT-5 cabling. Now signals can be exactly aligned at the receiver for a razor-sharp image.



Video transmitted over 1000 feet of CAT-5. Note the lack of alignment on the RGB test pattern.

EL9115 is programmed to align the RGB vertical test bars. De-skewing required 44ns delay on green and 18ns on red. The test bars now line up vertically.

NEW - EL9111 and EL9112 Tripple Signal equilizers offer even more design flexibility.



Features

- 62ns total delay
- 2ns delay step increments
- Operates from ±5V supply
- Up to 100MHz bandwidth
- Low power consumption
- 20-pin QFN package

Applications

- Video security systems
- KVM
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Complete Video Equalization and Compensation Solution

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The LeCroy units essentially rewrote the book on how engineers design these ultrawide-bandwidth instruments (70 to 100 GHz, depending on the manufacturer). At the product introduction, LeCroy referred to its instruments simply as sampling scopes, because "sequential" didn't really apply. But the problem with not qualifying "sampling" is that all digital scopes are sampling scopes. During the year, LeCroy solved its terminology problem by inventing a new term, "NRO" (near-real-time oscilloscope) and adding an NRO series to its line.

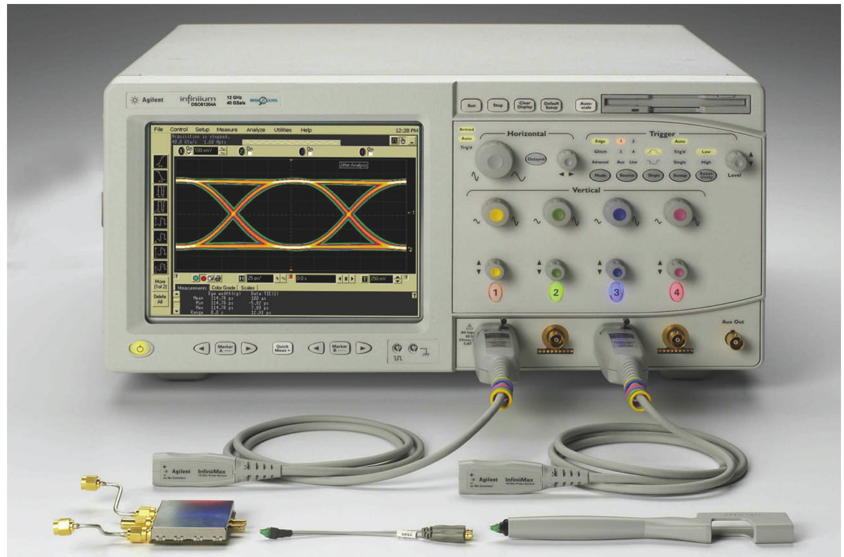
All scopes in this category—including the LeCroy units—depend on the signal's occurring repetitively. It need not recur at a constant rate, but it must follow a trigger signal by an essentially fixed delay. Classic sequential-sampling scopes capture only one sample during each iteration of the input waveform, advancing the sampling point incrementally with each new trigger. Thus, despite their extremely wide bandwidth, these scopes acquire waveforms slowly. This low speed rules out instruments of this type in many common scope applications.

In some of these scopes, the analog sampler is separate from the scope mainframe. The sampler is a so-called zero-order hold circuit, which captures the input signal with femtosecond aperture uncertainty and maintains the captured voltage for tens of microseconds. The sampler output is thus a relatively low-frequency replica of a multigigahertz signal. From the sampler output onward, the analog signals that the scope deals with are relatively low in frequency. The ADCs in such scopes are usually high-resolution (14 bits or more) successive-approximation devices with conversion rates no higher than a few hundred kilohertz. Memory depths in classic sequential-sampling scopes rarely exceed 100k samples.

BANDWIDTH TO 100 GHz

Advances in sampling technology enable the LeCroy units, with the appropriate sampling plug-ins, to achieve industry-leading 100-GHz bandwidth, whereas advances in ADC and memory technology make possible an architecture that differs considerably from that of sequential-sampling instruments. Instead of taking only one sample during each iteration of the input waveform, the LeCroy units take many. The company says that the sampling rate is 50 times that of the fastest competitive instrument. In addition, memory depths of hundreds of millions of samples are possible, and a built-in clock-recovery facility allows the scopes to operate, in many cases, without an external trigger. The scopes also accommodate built-in analysis features that you would probably expect to find only in real-time-sampling scopes. Thus, these scopes can handle many applications in which competitive instruments would acquire data too slowly, could not capture records of the necessary length, would require external equipment to trigger from the available signals, or would present a more complex interface to less-extensive analysis facilities.

As do Agilent and Tek, LeCroy offers optical-to-electrical converters to permit use of its ultrawideband scopes for fiber-optic communication-system measurements. Unlike its competitors, though, LeCroy does not currently offer differential-input plug-ins for these scopes. As a result, you need two of the LeCroy mainframes to simultaneously view four more-than-20-GHz differential signals—a task the competitive units can perform with one mainframe. EDN



Acquiring multigigahetz signals without introducing loading effects that completely invalidate the measurement requires great care, an understanding of the physics of probing, and highly specialized probes. These 10-GHz Infiniimax units from Agilent work with one of the company's DSO 80000-series scopes.

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AUTHOR'S BIOGRAPHY

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The Sonos ZonePlayer ZP80 is part of a Linux-based wireless system that streams digital music to audio equipment throughout a consumer's home.

BY WARREN WEBB • TECHNICAL EDITOR

LINUX joins the consumer-electronics REVOLUTION

DESIGNERS ARE TURNING TO THE LINUX OPERATING SYSTEM TO MEET THE ESCALATING USER-INTERFACE, NETWORKING, AND MULTIMEDIA REQUIREMENTS OF TODAY'S CONSUMER-ELECTRONICS PRODUCTS.

As CE (consumer-electronics) vendors vie for market share, consumers are asking designers to cram more functions into every new product or update. Users are no longer content with devices that offer only one function. Multifunction devices, such as mobile phones, media players, digital cameras, game consoles, radios, and televisions are all competing for consumers' dollars. To deal with this complexity, 32-bit processors, networking connections, full graphics displays, security, and multithread software are now standard fare in new designs. With the high volumes and thin profit margins associated with CE products, design teams are investigating and adopting the Linux operating system to tackle the software burden.

Several Linux features make it ideal for CE projects. Designers are initially attracted to Linux because it offers free source code, no licensing fee, and no per-unit royalties. Compared with the price of in-house development or a commercial operating system, these costs are significant and can add up to thousands of dollars over the life of the project. Cost competition and budget restrictions have forced software-development teams to at least consider royalty-free software such as Linux for new projects.

Linux includes the kernel, the shell environment, and applications. The basic architecture of the Linux kernel includes memory management, process scheduling, a file system, and a network interface. The memory manager enables multiple programs to securely share the system memory, and the process scheduler ensures that programs will have fair access to the CPU. The virtual-file system hides the details of the hardware and presents a common file interface to the user. The Linux kernel typically takes less than 1 Mbyte of RAM, and the shell environment pro-

AT A GLANCE

- With the price of 32-bit processors and memory plummeting, Linux fits a large portion of next-generation consumer-electronics devices.
- Designers can configure the Linux kernel for small-footprint systems and provide many features of a powerful operating system.
- Design teams that historically developed operating software in-house are turning to Linux to deal with increasing device complexity.
- Linux vendors make money by bundling subscription support, tools, and services with custom distributions.
- A large online community of Linux developers provides users with a ready source of technical experts and rapid problem resolution.

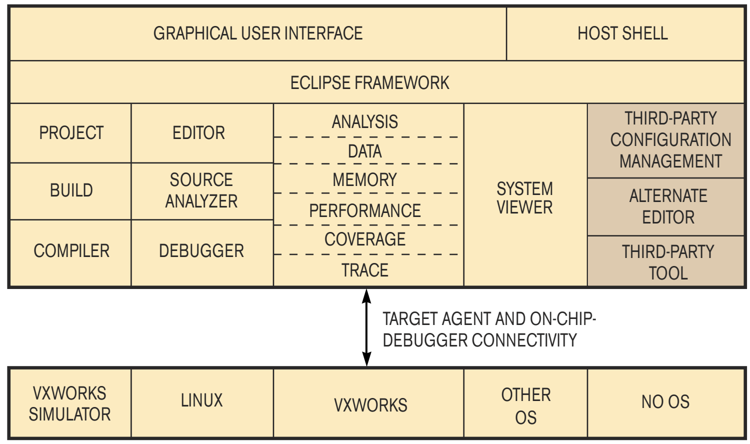

Figure 1 The Wind River Workbench suite integrates Linux and VxWorks design tools into the open-source Eclipse integrated development environment.

vides a user interface as simple as a command line or as complex as a Windows-type graphical interface.

Linux comes along at a time when some designers are moving from limited-function "roll-your-own" operating software for 8- and 16-bit processors to complex applications that exceed the capabilities or budgets of in-house software teams. These developers are accustomed to maintaining their own software packages and feel at home with the Linux licensing arrangement. Open-source Linux add-on features such as built-in networking support and graphics can also save many hours of coding and integration on a new development project.

With the current crop of high-speed, low-cost 32-bit processors and Linux pre-emption improvements, developers are finding that the real-time demands of embedded systems are less of a burden. Although data rates have increased, the timing of user I/O has remained relatively constant, and programmers have more clock cycles available to service I/O requests with today's high-speed processors. Linux does not target the delivery of deterministic performance, yet it is in use on some applications that previously required a real-time operating system.

LOW OVERHEAD

Linux is modular and allows developers to construct a small, tailored software set that fits the memory footprint of each device, thus eliminating some of the code overhead in proprietary, multiuse operating systems. Linux also supports a vast arsenal of microprocessors, making it ideal for the diverse consumer-device market. Because designers have ported Linux to most popular embedded processors, software limitations do not force developers into hardware decisions. Designers can start production with a low-priced microprocessor that meets current needs and

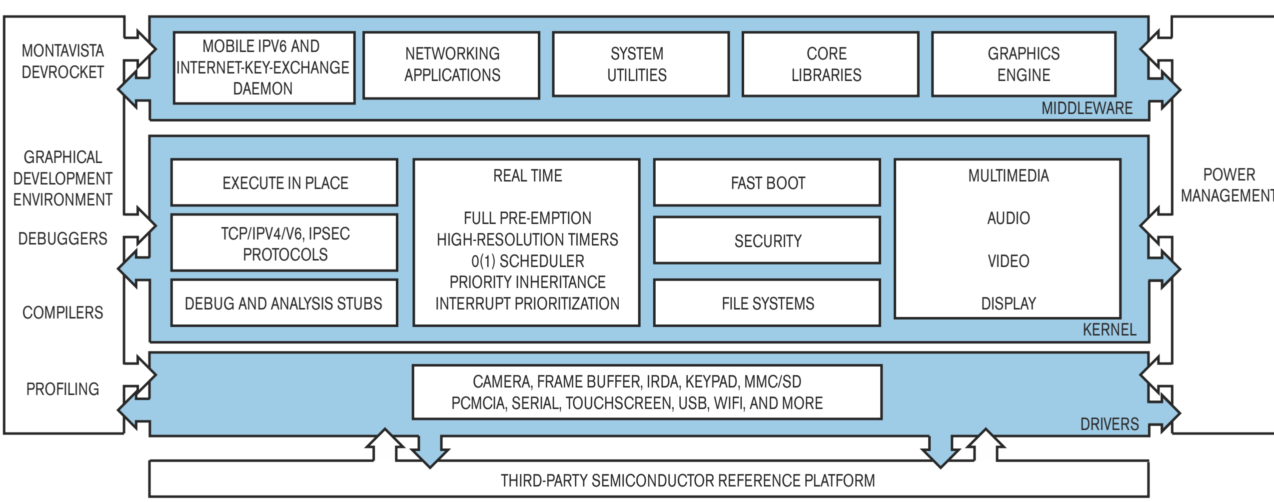

Figure 2 MontaVista Software offers the Linux Consumer Electronics Edition, a Linux operating system and cross-development environment for CE devices.

easily upgrade to a more powerful CPU as the device requirements and features expand.

Developers periodically update the Linux kernel to include patches and suggestions from the user community. You can find information on and download the latest version of the kernel at www.kernel.org. The current Version 2.6 includes numerous pre-emption points that allow the scheduler to suspend an active task and initiate a higher priority process. A rewritten process-scheduler algorithm speeds task switching in multitasking applications. In addition to the real-time improvements, Version 2.6 includes several updates that benefit consumer-device applications. For example, Bluetooth and USB 2.0 enhance peripheral-interface options, the ALSA (Advanced Linux Sound Architecture) allows applications to process multiple audio streams, and Video4Linux adds a video subsystem. Another update for deeply embedded systems yields a smaller footprint build for headless applications.

The Linux licensing agreement has positive and sometimes negative consequences for the consumer-device developer. On the positive side, you can download a free copy of Linux, adapt it to your product, and sell as many copies as you want without paying royalties. Linux is licensed under the GNU (GNU's Not Unix) GPL (General Public License) with rules for its use. If you modify and distribute GPL software, your modifications automatically fall under the GPL, and you must reveal the source code. Application programs and device drivers may remain proprietary as long as they are separate and distinct from the Linux kernel and contain no GPL code. The code-isolation requirement concerns developers of small-footprint consumer devices in which a single ROM image stores all software.

In addition to the licensing uncertainties, other nontechnical concerns exist for prospective Linux users. For example, the SCO (Santa Cruz Operation) Group's legal challenge claiming that Linux contains remnants of proprietary Unix code could force changes to the kernel or even require royalty payments. As recently as December 2005, the SCO Group filed a motion to expand a lawsuit against Novell, a previous owner of Unix intellectual property and a current Linux developer. You can find the latest information and a complete history of the SCO controversy at the Linux Online Web site, www.linux.org.

Figure 3 The $360 Nokia 770 Internet Tablet delivers wireless connectivity, an 800×480-pixel touchscreen, and 64 Mbytes of available flash memory.

KERNEL PATCHES

Another possible danger that developers foresee in an open-source Linux environment is the potential for fragmentation. If Company A decides to modify the Linux kernel to solve an integration problem with one of its products, and Company B makes a similar but incompatible modification, three versions of Linux now exist. When the next official Linux update comes out, both companies will have to dig through the revised code to reincorporate their changes or continue to use the old version. The wisest choice would be to leave the kernel unmodified and use the source code strictly for debugging or to gain insight into the internal functions of Linux. So far, the Linux community has been successful in preventing multiple versions through an elaborate system of upgrade proposals and releases.

Although Linux is a free operating system, many designers are willing to pay for expert support, specialized tools, customization services, and prepackaged configurations to ease the development process. Commercial vendors have responded with custom embedded configurations, subscription-support packages, development-tool kits, sample applications, and consulting services to augment Linux. Unlike with commercial proprietary operating systems that limit users to a single source, Linux users have the freedom to obtain support from any number of vendors.

Concerned with the growing popularity of Linux for CE products, some commercial RTOS (real-time-operating-system) vendors have joined the open-source movement to provide custom distributions, development tools, and support and to promote their proprietary software for hard-real-time applications. For example, Glenn Seiler, product-line manager at Wind River, summarizes the company's strategy: "The market wants a choice. In some cases, the market wants an RTOS because of hard-real-time or small-footprint requirements, and some customers still have an aversion to the GPL concept. Others have so much legacy investment that they want to continue to use the RTOS."

Seiler describes other customers who want to take advantage of the fast innovation, royalty-free model; have control over the source code; want vendor independence; and are unafraid of the GPL. These customers, he says, are leaning more toward Linux. He explains, "We wanted to provide a solution that would satisfy both the RTOS customer and the Linux customer. We started that solution with a tools strategy based on our Workbench tool suite: a soup-to-nuts, life-cycle product that covers everything from board bring-up and firmware development all the way to kernel-board-support development, application development, and debugging." Wind River based the Workbench suite on the open-source Eclipse integrated development environment (**Figure 1**).

Similarly, MontaVista Software offers the Linux CEE (Consumer Electronics Edition), an embedded operating system and cross-development environment for CE devices. The package features dynamic power management; enhanced file systems; new development tools for system-performance tuning; processor and peripheral support; cross-development tools for application development; and sample utilities, libraries, and drivers. CEE supports a range of consumer-device-specific processors from Freescale, Intel, Renesas, and Texas Instruments. Mon-

taVista also offers Linux for Mobile Devices (Mobilinux) for wireless handsets and mobile products with requirements for power management, hard-real-time performance, fast start-up, and small footprints (**Figure 2**).

TIVO LEADS THE WAY

Numerous CE devices incorporate the Linux operating system, but the TiVo personal video recorder is the most widely recognized. The TiVo Linux has also been hobbyists' favorite software to "hack" to increase storage capacity with larger or additional hard disks or to transfer video to computers or other devices. Linux may also be part of the software package that Sony provides with its next-generation gaming console, PlayStation 3, which Sony expects to ship in the spring of 2006. Linux also powers the recently introduced Nokia 770 Internet Tablet featuring 802.11, USB, and Bluetooth connectivity; an 800×480-pixel touchscreen; and 64 Mbytes of available flash memory (**Figure 3**). In addition to the Web browser, the 770 includes an e-mail client, media players, a file manager, games, and several general-purpose applications. The Nokia 770 is available online for $360.

At the recent Consumer Electronics Show in Las Vegas, Sonos introduced the Linux-based ZonePlayer ZP80, part of a wireless system that allows users to stream digital music to audio equipment throughout a consumer's home. By connecting a ZP80 to any amplified audio device using the analog or digital outputs, that device becomes part of a wireless, multiroom digital-music system that you operate from a color Sonos controller. The ZP80 includes autosensing line-in connectors that can digitally encode any line-in audio source, such as an Apple iPod, a CD player, or a satellite radio. The Sonos ZonePlayer ZP80 retails for $349.

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If you are new to Linux for CE, you can find news, discussion, and custom source code at the CELF (Consumer Electronics Linux Forum). The forum's goal is to enhance Linux functions for use in CE devices by publishing specifications and hosting CE-specific code. You can also find information on Linux-based CE products at www.linuxdevices.com. This site contains recent news, articles, and tutorials on Linux programming, lists of available distributions, and forums on embedded-system topics.

As next-generation CE devices come to market, designers must be ready to deliver complex user interfaces, network connections, and real-time data security on top of their custom application software. Linux offers a royalty-free, open-source operating system with these and other features built-in. In fact, millions of lines of free Linux-compatible software are available on the Internet to support CE-development projects. With these benefits and a growing base of technical fans, Linux has a bright future in the CE industry. **EDN**

You can reach Technical Editor Warren Webb at 1-858-513-3713 and wwebb@edn.com.

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Digitally Controlled Power

High Performance Analog Solutions from Linear Technology

There is considerable diversity under the "digital power" umbrella. Most solutions address the power supply telemetry needs of complex systems such as networking, telecom and high availability systems. Products supporting these applications provide digital communications, sophisticated monitoring and control of the power supply. Also under the "digital power" umbrella are power supply controllers that utilize digital processing within the regulation loop. Use of digital signal processing has been proposed at various times over the years. But the need for measuring load currents and voltages, the need for better than 1% regulation accuracy and the convenience of digital communication are driving the creation of integrated solutions specifically tailored for power supply applications.

Optimizing Digital Power for High Availability

Designed for digital management of power supplies in high availability systems, the LTC®2970 dual I²C power supply monitor and margining controller offers the best melding of digital and analog power. The I²C digital interface, 14-bit ADC, highly accurate reference and current output DACs (IDACs) give digital power supply designers what they want: digital control of an analog power

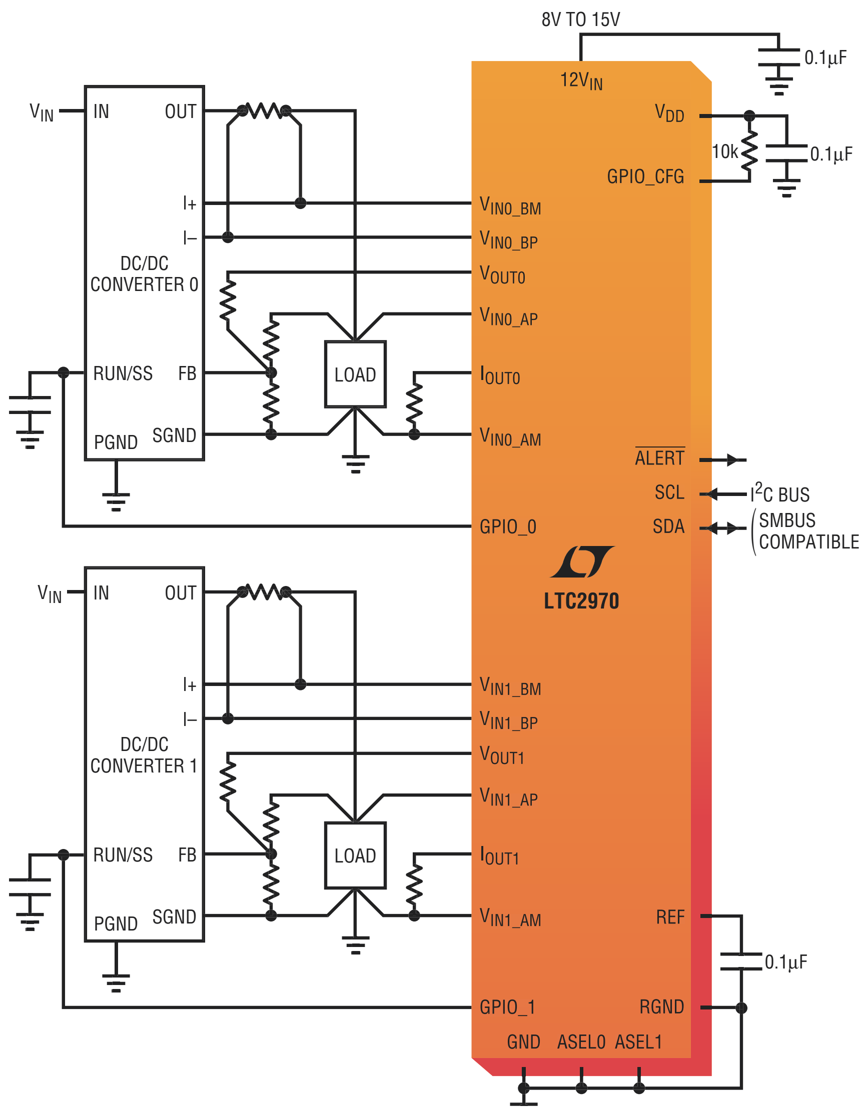

Figure 1. Dual I²C Power Supply Monitor and Margining Controller

Digitally Controlled Power

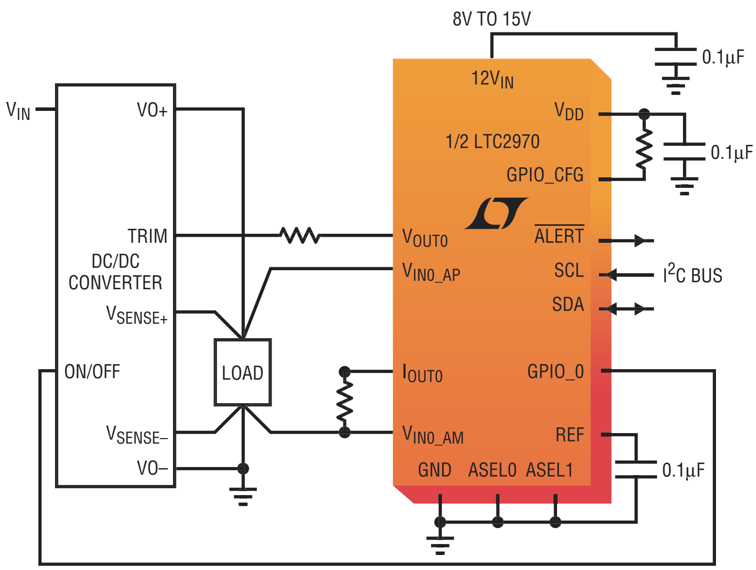

Figure 2. LTC2970 Application Circuit for DC/DC Converters with a TRIM Pin

supply. The LTC2970 works with most any power supply, allowing designers to choose the optimal DC/DC converter with an analog control loop that provides smooth control of the output voltage and fast transient response. An on-chip reference and 14-bit delta-sigma ADC ensure accurate measurements of supply voltages, load currents or temperature. Two voltage-buffered 8-bit IDACs adjust the DC/DC converters' feedback signal. The adjustment range and resolution is configurable using just two resistors per channel, and the IDACs can be programmed by a slow, linear voltage servo in order to accurately trim and margin the converters' outputs. This makes the LTC2970 useful in determining the sensitivity of the power supply during the prototype phase or in production to test for manufacturing variations.

The end products conducive to digital power management are equally likely to incorporate DC/DC modules, as they are to have IC-based converters. The LTC2970 is equally suited whether the DC/DC converter offers a TRIM pin or if it offers access to the feedback node. Figure 2 illustrates a typical application circuit for margining the output voltage of a DC/DC converter with a TRIM pin. Following power-up, the LTC2970's V_{OUT0} pin defaults to a high-impedance state. If the soft-connect feature is used, the LTC2970 will automatically find the IDAC code that most closely approximates the TRIM pin's open-circuit voltage before enabling the IDAC voltage buffer (see Figure 4).

Accurate Power on Demand

Need something better than the typical 1.5% to 2% regulation offered by today's DC/DC converters? Need to move the voltage down 100mV to hit the "sweet spot" of your brand new ASIC? Don't know where that "sweet spot" is yet? You need accurate power on demand. You need the LTC2970.

The superior accuracy and ultralow drift of the on-chip reference, combined with the 14-bit delta-sigma ADC, provide better than ±0.5% total unadjusted error in the voltage measurement. Feeding the measured value back and tweaking the DC/DC feedback node with an 8-bit DAC creates a servo mechanism to program the DC/DC output voltage with extreme accuracy. The LTC2970 can do this for you! Program an output voltage and it will automatically seek that value, iterating one LSB at a time for a monotonic approach to the final voltage. You can easily margin up, margin down or set a new value (see Figure 3).

The LTC2970's delta-sigma architecture was specifically chosen to average out power supply noise and allow the LTC2970 to ignore fast transients. The DC/DC converter attributes are chosen for transient response, whereas the LTC2970 is selected for accurate voltage programming. The device offers additional telemetry functions due to the range of inputs to the ADC. The LTC2970 uses differential inputs to precisely servo supply voltages regardless of ground offsets. The device has additional differential inputs to measure current and to monitor the supply voltage, as well as the internal die temperature.

The LTC2970's current output DACs provide smooth, continuous control of the feedback node. Unlike discrete time or PWM output DACs, the LTC2970's continuous time, voltage-buffered, current output DAC is ideal for noise-sensitive applications. Connection of the current output to a unity gain voltage buffer is switched, allowing the DC/DC converter to come

Telemetry Functions

Measure output voltage	Flag Under/Over-voltage (user set)
Measure output current	Flag Under/Over-voltage (user set)
Measure LTC2970 die temperature	Measure LTC2970 supply voltage

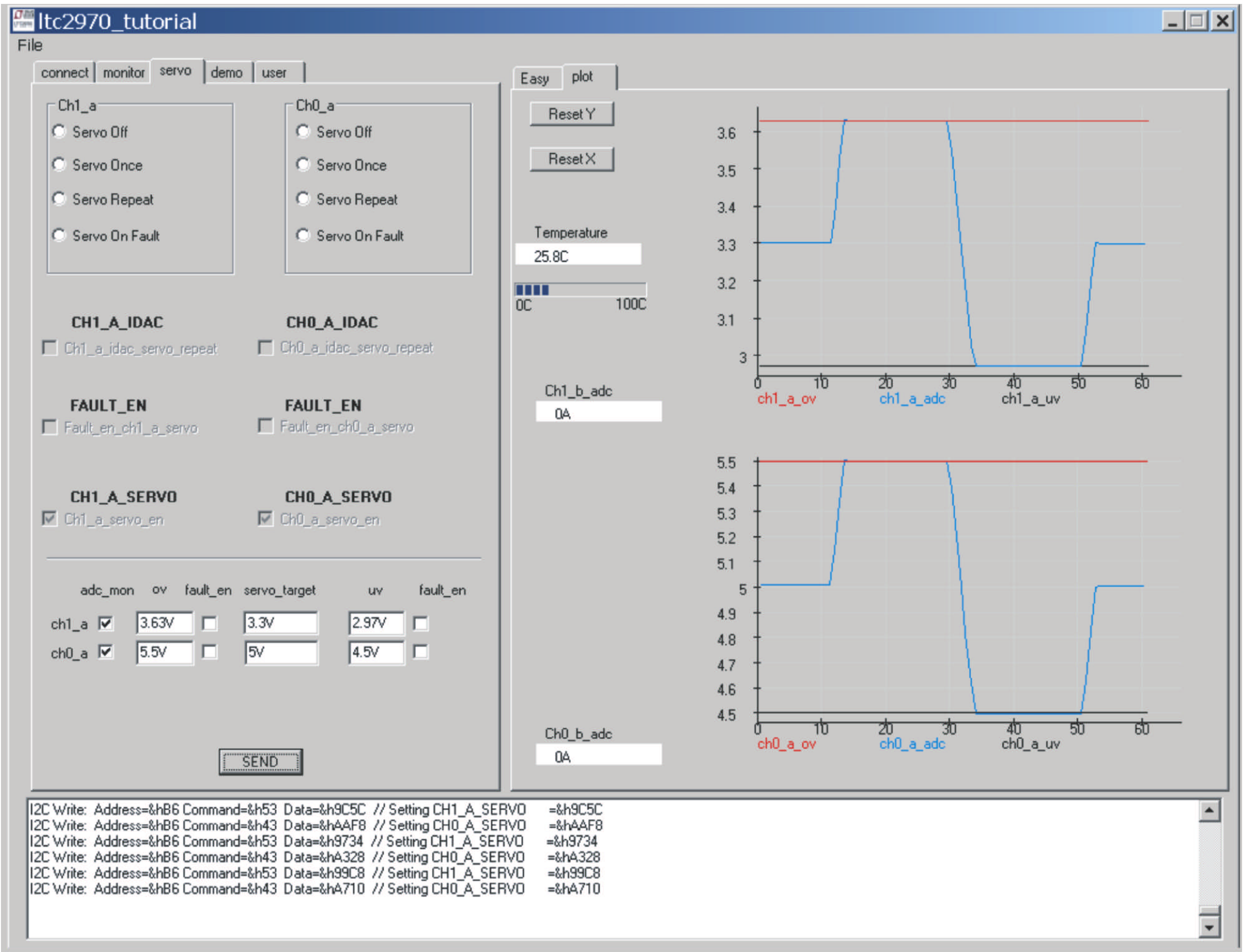

Figure 3. Demonstration System Showing Automatic Margining Capability

up and stabilize prior to engaging the servo control (Figure 4). The voltage buffer switch is isolated from the LTC2970's V_{DD}, so the DC/DC converter operation will not be impaired if the LTC2970 is unpowered. Selecting the proper resistor value between the I_{OUT} node and ground sets the maximum voltage range limit beyond which the supply cannot be driven. The V_{OUT} node then supplies current to the feedback node through a series resistor. The buffer can be connected in two ways: beginning with a point equal to the nominal regulation value (soft connect), or immediately with the programmed, final value (hard connect). The ground reference for the DAC can be set at the point of load, minimizing errors due to ground bounce.

Tracking and Sequencing with the LTC2970-1

The LTC2970-1 enables power supply tracking and sequencing with the addition of a few external components. A special global address and synchronization command allow multiple LTC2970-1s to track and sequence multiple pairs of power supplies.

A typical LTC2970-1 tracking application circuit is shown in Figure 5. The GPIO_0 and GPIO_1 pins are tied directly to their respective DC/DC converter RUN/SS pins. When GPIO_CFG is pulled-up to V_{DD}, the LTC2970-1 will automatically hold off the DC/DC converters after power-up by asserting open drain outputs GPIO_0 and GPIO_1 low. N-channel FETs Q10/11 and diodes D10/11 form unidirectional range switches around resistors R30A/31A while GPIO_CFG is high. These range switches allow the LTC2970-1's V_{OUT0} and V_{OUT1} pins to drive the converter outputs all the way to/from ground through resistors R30B/31B. When GPIO_CFG

Digitally Controlled Power

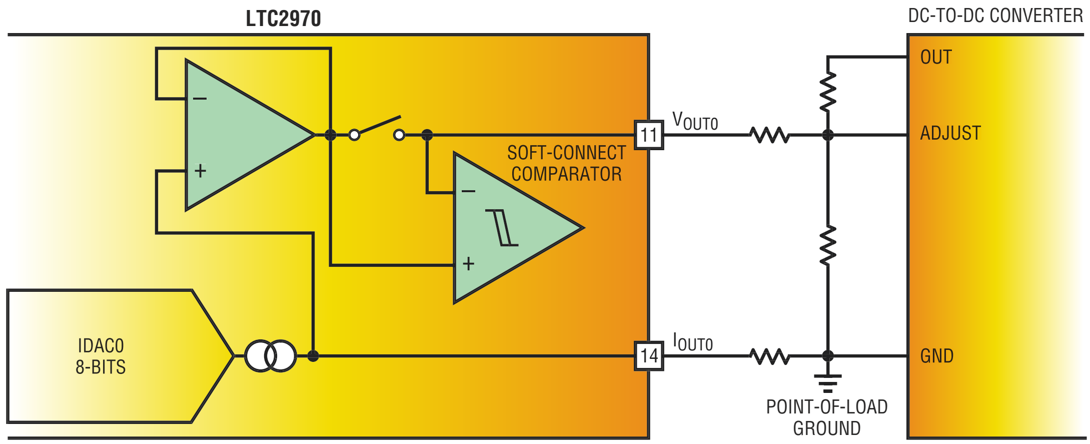

Figure 4. Configuring the DAC Outputs

pulls low, N-channel FETs Q10 and Q11 will turn off. R30A/31A and R30B/31B then combine in series for normal margin operation. The 100k/0.1µF low-pass filter in series with the gates of Q10/11 minimizes charge injection into the feedback nodes of the DC/DC converters when GPIO_CFG pulls low.

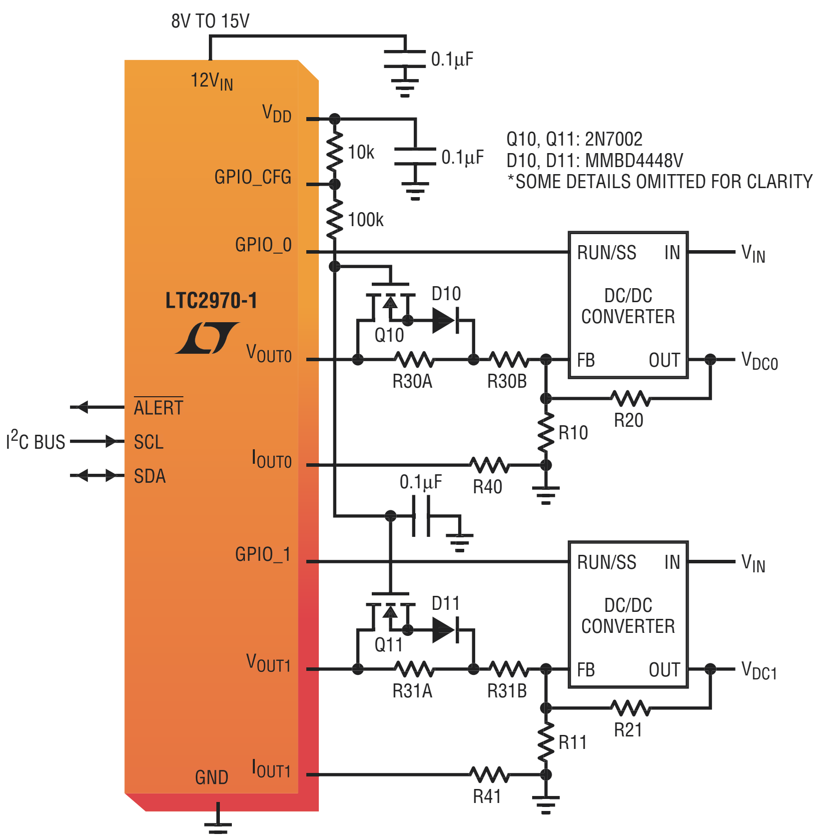

Figure 5. Using the LTC2970 to Track Two Supplies

Digital Communications

All communication with the LTC2970 is performed over an industry standard I^2C bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines. The LTC2970 I^2C interface also meets all SMBus setup times, hold times, and timeout requirements. The $\overline{\text{ALERT}}$ pin may be used to signal that one or more of the fourteen configurable fault limits have been reached. Each fault may be individually masked. The I^2C interface supports word reads, word writes and the SMBus Alert Response Address protocol. Two general purpose IO pins may be used to provide additional fault information or user-defined system control. Powering down the LTC2970 will not interfere with I^2C operation.

Conclusion

The LTC2970 provides a highly accurate digital power solution for digital communications, sophisticated monitoring and control of the power supply. Choose the optimal DC/DC converter for your application, and then add the LTC2970 for the best of both worlds.

BY GLEN BRISEBOIS • LINEAR TECHNOLOGY CORP

Signal conditioning for high-impedance sensors

MAINTAINING ACCURACY IN CIRCUITS THAT PROCESS SIGNALS FROM HIGH-IMPEDANCE SENSORS PRESENTS UNIQUE CHALLENGES. FIRST, YOU NEED TO IDENTIFY WHEN TO USE SPECIAL DESIGN TECHNIQUES. THEN, YOU MUST CHOOSE DEVICES THAT BUFFER AND PROTECT THE SENSORS AND CIRCUITS WITHOUT DESTROYING THEIR ACCURACY.

If you had the option, you probably wouldn't use high-Z (high-impedance) sensors. Their sensitivity to external noise, solder-flux residue, particle tracking, bias currents, and distant charges can make repeatable measurements difficult. High-Z sensors have an upside, though: They don't self-load, and they inherently use little power. For certain variables, such as pH, light, acceleration, and humidity, the most practical sensors are high-Z devices. Because nature offers them, expediency urges their use. Careful attention to design can minimize the devices' tendency to receive adverse effects from the world around them. As an interesting note, with the advent of practical superconduction, impedance values have achieved an infinite range.

When you make measurements to characterize the behavior of any circuit that processes signals from high-Z sensors, you should drive the circuit's inputs through a high Z or a high resistance. Every engineer who works with signal conditioners for high-Z sensors should have some high-value reference resistors at hand. Vishay (www.vishay.com) offers surface-mount resistors with values to 50 GΩ. Samples with values of 1 and 2 GΩ were available off the shelf at press time. The Mini-Mox series from Ohmite (www.ohmite.com) contains leaded 10- and 100-GΩ resistors. All of these high-value resistors are remarkably "stiff" (conductive, nonisolating). For example, a colleague warns users not to touch the resistor bodies, lest skin-oil deposits reduce the impedance.

This warning suggested an experiment. Connecting a Keithley (www.keithley.com) Model 614 electrometer across the resistor leads resulted in a meter reading of 9.9 to 10 GΩ. After thoroughly touching and squeezing the resistor body from lead to lead with oily fingers and then backing away, the meter returned to precisely where it had been: 9.9 to 10 GΩ. This test shows only that skin oils are not an immediate threat to these resistors. To ensure reliability over time and humidity, sound laboratory practice still exhorts keeping components, pc boards, and insulators clean. Skin-oil conductivity is known to vary among individuals. For cleaning, Ohmite recommends using isopropyl alcohol and lint-free wipes and baking the device at 75°C for one hour to drive off moisture. When performing an impedance measurement of this type, bear in mind that the insulator in the cable is entirely in parallel with the resistor under test. Limiting error to 1% in a 100-GΩ-resistor measurement requires an overall insulator impedance of no less than 10 TΩ. The only way around this limitation is to perform an open-circuit calibration to measure and mathematically remove any shunt resistance. The Keithley 614 lacks this feature, but it still performs well, reinforcing the idea that, compared with an insulator, a 10-GΩ resistor is indeed relatively stiff.

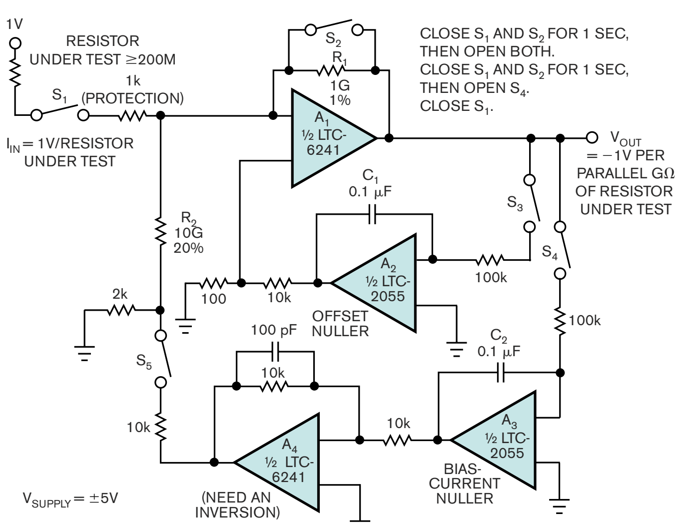

Figure 1 Using nulling techniques is tempting, and you can sometimes make them work with much effort and shielding. But making a "perfect" amplifier like this one becomes expensive and departs from the high reliability of solid-state design. You may be bankrupt before your design reaches production.

ENEMIES OF HIGH-Z CIRCUITS

When Z is high, leakages, current noise, bias currents, and static voltages dominate the errors, so dealing with high-Z circuits means minimizing those quantities. The most common and addressable form of leakage is solder-flux residue. Carefully clean any board that supports high-Z circuits to remove all flux. Washers that board manufacturers use can be contaminated. Space traces beyond the minimum design rules to the extent that board area allows. For insulators, FR-4 usually causes no problem, although, unlike Teflon and glass, it does absorb moisture. Some designers have had success with Teflon posts or wells, but the good results may be due to these components' inherent resistance to surface tracking and other effects, such as dielectric absorption, rather than their purely insulating properties. Keeping surface impedances high in imperfect environments may require sealing or conformal coating, but such measures can reduce serviceability. Guard traces connect to high-Z sources with traces at similar potentials. Through-hole pins should have guard traces on all or at least on the outside layers. There are many practical considerations. For example, a dual op amp has noninverting inputs on pins 3 and 5. It is easier to guard Pin 5, because it is in the corner; Pin 3 is next to the negative supplies.

Bias current and current noise in active devices are sources of error. Bipolar transistors require dc base currents to operate; FETs have input leakage. In both cases, electron quantization through junctions induces current noise. (Such noise is present only in currents that flow through junctions.) In FETs, current noise rises with frequency because of Miller effects (see **sidebar** "Current-noise measurements" with the Web version of this article at www.edn.com/ms4177). Although you may want to jump immediately to FET-based input structures for their low bias currents, superbeta bipolar input structures can offer advantages, particularly in high-temperature operation. FET-input leakage doubles every 10°C, whereas superbeta bias current remains relatively stable. In either case, chopping techniques can remove the effects of both offset voltage and bias current. For impedances of less than a few megaohms, don't jump immediately to a FET-input amplifier without first considering exceptionally precise, low-bias-current op amps, such as Linear Technology's LT6010 or LTC2054. Sometimes, a lower offset voltage can be more important than a lower bias current.

For a given source impedance, the overall input error is $V_{OS}+I_{BIAS}\times R_{SOURCE}$. As the source impedance rises, the bias-current term dominates, making a MOSFET input more attractive. MOSFET inputs have in recent years gained popularity as CMOS-op-amp specifications have improved.

Another problem with high-Z circuits is their sensitivity to motion. Shoes rubbing against a carpet can generate static charges that can reach kilovolt levels, so even the tiniest capacitive coupling can inject significant charge. When taking measurements, stand back and hold still. Shielding helps, of course, but mechanical vibrations (microphonics) modulate the capacitance between pc-board traces and any local metalwork, causing charge injection—even if the metalwork does not change in voltage but simply stays at a dc voltage different from that of the traces. So shield your circuit, but not too closely.

When mechanical motion or stress induces tiny voltages on insulators, triboelectric or piezoelectric effects occur. In high-vibration environments, high-Z sources may require low-triboelectric-noise cable, such as Belden (www.belden.com) type 9239.

DEVICE AND AMPLIFIER CONSIDERATIONS

Although discrete MOSFETs offer poor leakage specifications, the devices can outperform their specifications by as many as six orders of magnitude. The familiar 2N7002, for example, specifies maximum channel leakage of 1 mA and gate leakage of 0.1 mA. But if you look at these devices in the lab with 20V on

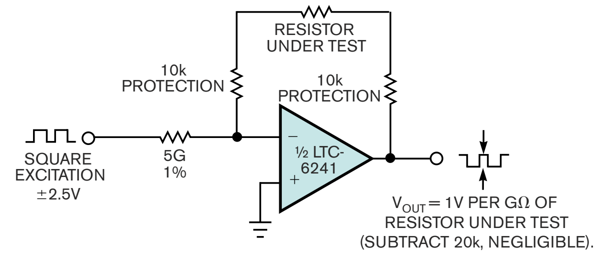

Figure 2 You can more easily achieve similar accuracy with chopped-excitation techniques. The amplifier's characteristics are not enhanced but rather measured and subtracted. What are the op amp's offset and bias current? It doesn't matter much.

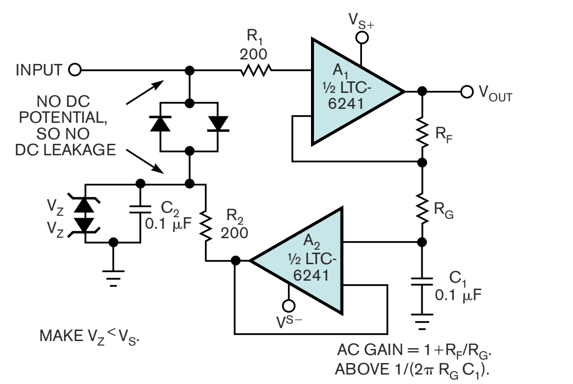

Figure 3 The tracking clamp has protection diodes, but A_2 back-drives them to the same voltage as the input. The zener diode and its capacitor carry most of the clamp current. R_1 and R_2 keep current away from the amplifiers.

the drain and a grounded gate and source, you find a total combined leakage of only about 1 pA. Obviously, the specifications do not reflect what the device does, but rather the cost of production-test time. Tighter specifications require more test time and better test equipment, for which you pay. Of course, tighter specifications also tend toward lower yield; you pay for that, too.

Ultralow-leakage matched-pair JFETs include the LS830 from Linear Integrated Systems (www.linearsystems.com) and the IFN124 from InterFET (www.interfet.com). A favorite single JFET is the Philips (www.semiconductors.philips.com) BF862 because of its 3-pA gate current, its subnanovolt noise density, and its easy-to-deal-with 0.6V pinch-off voltage. The 2N4416 is also popular, especially for its subpicofarad input capacitance and respectable noise density, but many designers have found troublesome JFETs' large and widely varying 2 to 6V pinch-off voltage.

CMOS op amps have for many years been available, but the specifications have been poor, and the actual results, even worse. Linear Technology has just introduced the precision micropower LTC6078 and the higher speed LTC6241 CMOS op amps. The LTC6241 offers a typical input-leakage current of 4 pA at 70°C. JFET-input-based electrometer-grade op amps have for many years been on the market but are relatively expensive. In the end, no op amp or semiconductor device is perfect, and some designers find that they can achieve the best dc results with relays and calibrating or chopping techniques.

Analog Applications Journal
BRIEF

Getting the most out of your instrumentation amplifier design

By Thomas Kugelstadt • Senior Systems Engineer, Industrial Systems

Introduction

Many industrial and medical applications use instrumentation amplifiers (INAs) to condition small signals in the presence of large common-mode voltages and DC potentials. Standard INAs using a unity-gain difference amplifier in the output stage, however, can limit the input commonmode range significantly. Thus, commonmode signals induced by adjacent equipment, as well as large differential DC potentials from differently located signal sources, can increase the input voltage of the INA, causing its input stage to saturate. Saturation causes the INA output voltage, although of wrong value, to appear normal to the following processing circuitry. This could lead to disastrous effects with unpredictable consequences.

This article reviews some principles of the classic three-op-amp INA and provides design hints that extend the input commonmode range to avoid saturation while preserving overall gain at maximum value. The article also discusses the removal of large differential DC voltages through active filtering, avoiding passive RC filters at the INA input that otherwise would lower its common-mode rejection ratio (CMRR).

INA principles

Figure 1 shows the block diagram of the classic three-opamp INA. The inputs, V_{IN+} and V_{IN-}, are defined through the input polarities of the difference amplifier, A3.

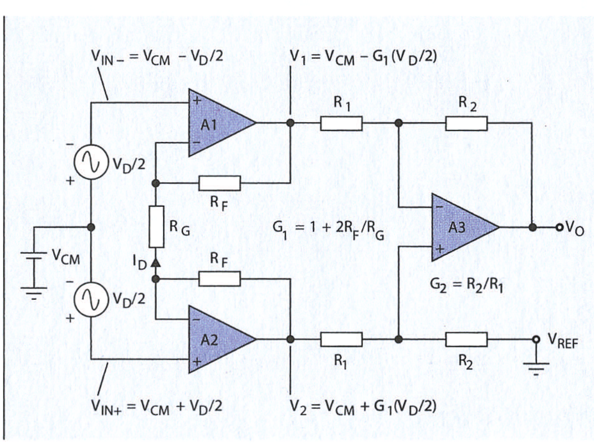

Figure 1. Classic three-op-amp INA and its voltage nodes

By definition, the INA's input signals are subdivided into a common-mode voltage, V_{CM}, and a differential voltage, V_D. While V_{CM}, the voltage common to both inputs, is defined as the average of the sum of V_{IN+} and V_{IN-}, V_D represents the net difference between the two.

$$\text{(1)}\quad V_{CM} = \frac{V_{IN+} + V_{IN-}}{2} \text{ and } V_D = V_{IN+} - V_{IN-}.$$

Solving both equations for V_{IN+} or V_{IN-} and equating the received terms results in a new set of equations, which, when solved for either input voltage, yields

$$\text{(2)}\quad V_{IN+} = V_{CM} + \frac{V_D}{2} \text{ and } V_{IN-} = V_{CM} - \frac{V_D}{2}.$$

In the nonsaturated mode, the op amp action of A1 and A2 applies the differential voltage V_D across the gain resistor, R_G, generating the input current, I_D:

$$\text{(3)}\quad I_D = \frac{V_{IN+} + V_{IN-}}{R_G} = \frac{V_D}{R_G}.$$

The output voltages of A1 and A2 are therefore

$$V_1 = V_{CM} - \frac{V_D}{2} - I_D R_F \text{ and } V_2 = V_{CM} + \frac{V_D}{2} + I_D R_F.$$

Replacing current I_D with Equation 3 yields

$$\text{(4)}\quad V_1 = V_{CM} - \frac{V_D}{2} G_1 \text{ and } V_2 = V_{CM} + \frac{V_D}{2} G_1,$$

where $G_1 = 1 + 2\frac{R_F}{R_G}$.

Equation 4 shows that only the differential component, $V_D/2$, is amplified by the input gain, G_1, while the commonmode voltage, V_{CM}, passes the input stage with unity gain. The difference amplifier, A3, subtracts V_1 from V_2 and amplifies the difference with the gain G_2:

(5) $$V_O = (V_2 - V_1)G_2, \text{ where } G_2 = \frac{R_2}{R_1}.$$

Inserting Equation 4 into Equation 5 and solving for V_O/V_D provides the transfer function of the INA:

(6) $$\frac{V_O}{V_D} = G_1 G_2 = G_{TOT}.$$

Extending the input common-mode voltage range

Note that V_1 and V_2 in Equation 4 do not represent absolute voltages. Because V_{CM} and V_D can change their polarities, the maximum voltage either output can assume before reaching saturation is

$$\pm\left|V_{1,2}\right| = \pm\left(\left|V_{CM}\right| + \left|\frac{V_D}{2}\right|\right) \leq \pm\left|V_{SAT}\right|.$$

For clarification, the following description simply ignores signal polarities, and the variables refer only to magnitude values. Assuming that $V_{1,2}$ and $V_D/2$ are constant, the only way to increase the input common-mode voltage from V_{CM} to V_{CM}' is to reduce the input gain from G_1 to G_1' so that

$$V_{1,2} = \text{constant} = V_{CM} + \frac{V_D}{2}G_1 = V_{CM}' + \frac{V_D}{2}G_1'.$$

Solving for V_{CM}' yields

$$V_{CM}' = V_{CM} + \frac{V_D}{2}\left(G_1 - G_1'\right).$$

Reducing G_1 reduces the range of the amplified differential component, G_1' ($V_D/2$), thus providing an expansion range for V_{CM}. Standard INAs, using unity-gain difference amplifiers, have $R_2 = R_1$ and $G_2 = 1$.

The total INA gain is then placed into the input stage, making $G_1 = G_{TOT}$. Equation 6 shows that reducing G_1 from G_{TOT} to G_1', while preserving G_{TOT}, requires an increase in difference amplifier gain from $G_2 = 1$ to $G_2' = G_{TOT}/G_1'$.

(7) $$V_{CM}' = V_{CM} + \frac{V_D}{2}G_{TOT}\left(1 - \frac{1}{G_2'}\right)$$
$$= V_{CM} + \frac{V_D}{2}G_1'\left(G_2' - 1\right).$$

Replacing G_1 with G_{TOT} and G_1' with G_{TOT}/G_2' results in the extended common-mode range:

This improved common-mode range at the amplifier output is now passed on 1:1 to the input. Applying gain to the difference amplifier requires access to the feedback resistor of A3 in Figure 2. A common solution uses a stand-alone difference amplifier, which provides access to the feedback resistor via a V_{SENSE} pin. The input stage is then realized by a dual low-noise amplifier, with external resistors R_F and R_G being used to set the input gain.

To raise the gain of a unity-gain amplifier, external resistors can be switched in series to R_2. However, the internal resistor values must be measured, as they can deviate by ±30% from their nominal values given in the datasheet. This approach works well for moderate gain. For large gain, however, the external resistors can reach prohibitive values, increasing noise to an undesirable level. A buffered voltage divider in the feedback path of A3 is then required.

Resistors R_3 and R_4 allow a wide range of gain settings with moderate resistor values. Voltage follower A4 provides low output impedance, which preserves the high CMRR of the difference amplifier.

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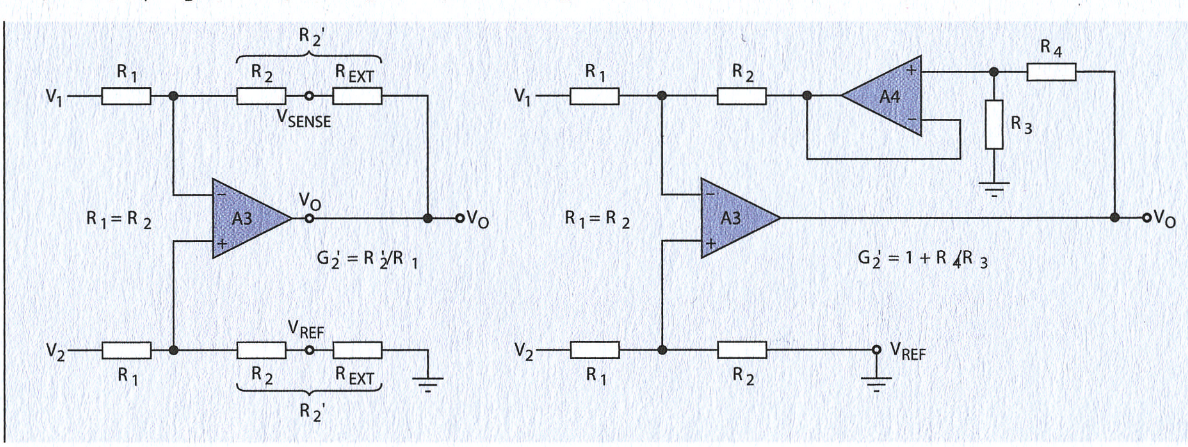

Figure 2. Increasing difference amplifier gain via REXT or buffered voltage divider

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The circuit in **Figure 1** incorporates two force-balance nulling techniques. To follow the operation, assume that all the switches are open and then close S_2 and S_3, thereby engaging ultraprecision integrating amplifier A_2 and forcing A_1's output to ground. A_1's input offset appears at its positive input, and C_1 stores 101 times this offset. Opening S_3 allows A_1 to function normally again, but with 1 mV of effective offset and approximately 1 mV/sec of drift. Now, opening S_2 puts feedback resistor R_1 in the circuit and causes an output voltage equal to $I_{BIAS} \times R_1$—typically, 1 mV. Closing S_4 and S_5 nulls A_1's output again, but this time through A_3. A_1's bias current now goes through R_2, and C_2 stores it as a voltage at 60 mV/pA. Opening S_4 ends the nulling phase.

Closing S_1 connects the input drive—the resistor under test—and a voltage source. Although the amplifier is now nearly perfect, it doesn't remain so for long. Drift on capacitors C_1 and C_2 requires a new nulling phase within several seconds; otherwise, the amplifier's specifications may degrade beyond those of an unaided LTC6241. **Figure 2** shows a simpler method. Rather than trying to perfect the amplifier, this circuit instead chops the excitation to allow subtraction of the amplifier contributions. Also, the resistor under test is now in the feedback path, so the output is proportional to the resistor's resistance rather than its admittance. Rise time is 10 msec (10 to 90%) with a 1-GΩ resistor, so the excitation should be no faster than about 10 Hz to ensure adequate settling.

PROTECTING A HIGH-IMPEDANCE CIRCUIT

How can you protect a high-Z circuit without affecting its input impedance? Strictly speaking, you can't, but you can come close. One of the best ways is to use a series resistor and some series inductance, even if it's just a length of trace. The inductance and parasitic elements spread out an ESD (electrostatic-discharge) pulse and improve the odds that it will jump to a chassis before it gets to anything sensitive. You can further improve those odds by introducing a spark gap in the layout near the connector pin to be struck. This approach is cheap and effective, but it can cause problems in higher density digital designs. The spark gap re-emits a strong EMI (electromagnetic-interference) wave, including some eerie blue. This phenomenon repeatedly crashed an onboard but distant 486 microprocessor, fortunately without harming the hardware. The protection you require depends on the level of immunity you specify for the design. In this case, the spark gap is a failure, because designers did not allow for PC-reset interventions. For analog designs or simple digital designs, spark gaps should not be a problem. Gas-discharge tubes, which are also available as components, are other alternatives.

Almost anything you do with diode clamps can cause leakage. Schottky diodes are probably out of the question because they tend to leak more. Ultralow-leakage diodes include the CMPD6001 series from Central Semiconductor (www.centralsemi.com) and the BAS416 from Philips. But the maximum-leakage specification, even when devices are cold, is 500 pA to 5 nA. The high-temperature specifications are even worse, often running into microamps. For the lowest leakage performance, JFET junctions still outperform diodes. The 2N4393, available from Vishay in an SOT-23 package, typically leaks 5 pA at room temperature and 3 nA at 100°C (**Figure 3**). Compare this leakage with the maximum-specified bias current of 75 pA at 70°C for the LTC6241. Adding even good diodes can cause a significant degradation. Some design work can help offset this problem, however. For example, consider the tracking-limiter circuit (**Figure 3**). A_2 back-biases the diodes, and C_1 stores the average dc voltage. The system shunts overvoltages and spikes to the reservoir capacitor but allows dc through with unity gain, protecting the inputs and improving input-overload-recovery time. For dc gain, simply short C_1 and move the input from A_2 to A_1's inverting input; inverting circuits are easier to protect, because you can simply connect the diodes to ground.

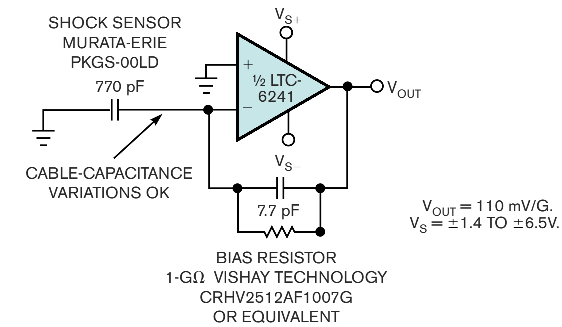

Figure 4 In this classic inverting-charge amplifier, variations in cable capacitance—that is, length—do not affect the signal gain. Use this circuit when the accelerometer is remote from the amplifier and the cable length is unspecified. Drawbacks are that the low-valued feedback capacitor sets the gain, and the bias resistor working into the same feedback capacitor determines the low-frequency performance.

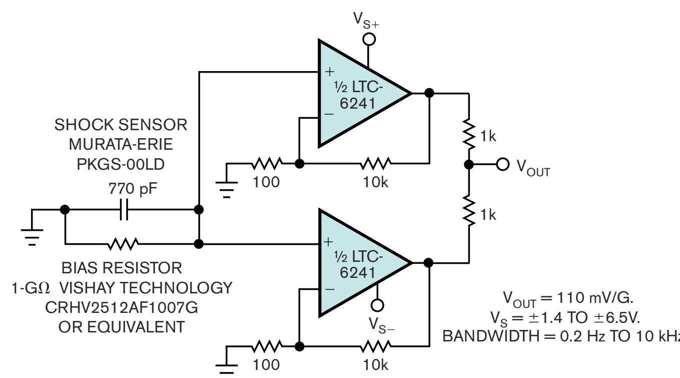

Figure 5 This noninverting-charge amplifier offers two advantages: You can connect stages in parallel to reduce voltage noise, and the bias resistor works into higher capacitance for better low-frequency response.

HOW HIGHER Z HELPS

Figures 4 and **5** show two approaches to amplifying signals from a capacitive sensor. The sensor in both cases is a 770-pF piezoelectric shock-sensor accelerometer, which generates charge under physical acceleration. **Figure 4** shows the classic charge-amplifier approach. The op amp is in the inverting configuration, so the sensor looks into a virtual ground. The op-amp action forces all of the charge the sensor generates

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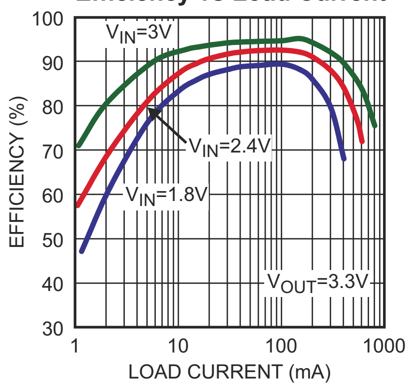

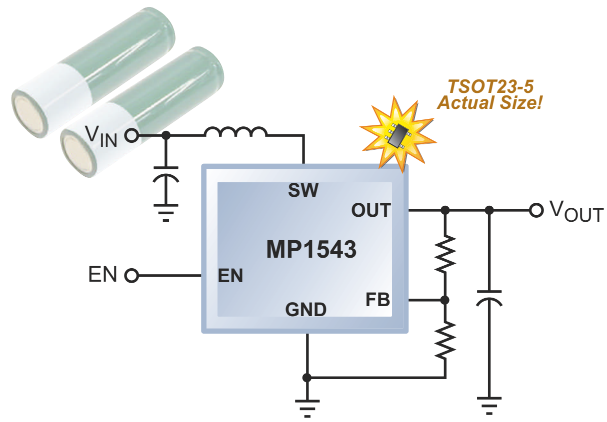

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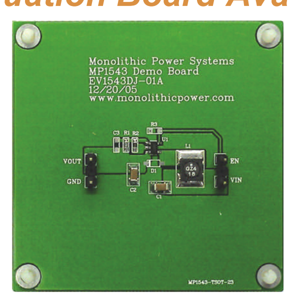

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across the feedback capacitor. Because the feedback capacitance is 0.01 times the sensor capacitance, the voltage across the feedback capacitor is 100 times what would have been the sensor's open-circuit voltage. So, the circuit gain is 100. The benefit of this approach is that the circuit's signal gain is independent of any cable capacitance between the sensor and the amplifier. Hence, designers favor this circuit for remote accelerometers whose cable length may vary. Difficulties with the circuit are inaccuracy of the gain setting with the small capacitor and low-frequency cutoff because the bias resistor works into the small feedback capacitor.

Figure 5 shows a noninverting-amplifier approach. This approach has many advantages. First, resistors, rather than a small capacitor, accurately set the gain. Second, the low-frequency response improves because the bias resistor working into the large 770-pF sensor, rather than into a small feedback capacitor, dictates the cutoff frequency. Third, you can sum and make parallel the noninverting topology for scalable reductions in voltage noise. This circuit's only drawback is that the parasitic capacitance at the input slightly reduces the gain. This circuit is a good fit for applications in which parasitic input capacitances, such as traces and cables, are relatively small and invariant.

When you calculate the bias resistance for the desired low-frequency cutoff, consider that you may want to make the bias resistor's value still larger. Doing so reduces the noise floor at low frequencies. For example, if you want to support frequencies as low as 10 Hz at −3 dB, the bias resistor works out to $1/2\pi \times 10\ \text{Hz} \times 770\ \text{pF} = 20\ \text{M}\Omega$. At 10 Hz, the 20-MΩ resistor contributes 580 $\text{nV}/\sqrt{\text{Hz}}$ of noise, which is 3 dB down, just like the signal. If you make the resistor value 1 GΩ, the accelerometer capacitance effectively attenuates the resistor's 4000-$\text{nV}/\sqrt{\text{Hz}}$ noise to 80 $\text{nV}/\sqrt{\text{Hz}}$, but the signal is barely attenuated. Sometimes, impedance higher than that normally required actually helps.

Devices and materials are available to support and protect high impedances. Dealing with high impedance requires a knowledge of what are otherwise minuscule phenomena. Sometimes, quantization of phenomena such as current noise can be challenging, but with the right circuit techniques, measurements become meaningful and repeatable. A proper breakdown of error sources, such as leakage, settling time, voltage noise, and current noise, helps the circuit designer to know what to expect. EDN

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ACKNOWLEDGMENT

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AUTHOR'S BIOGRAPHY

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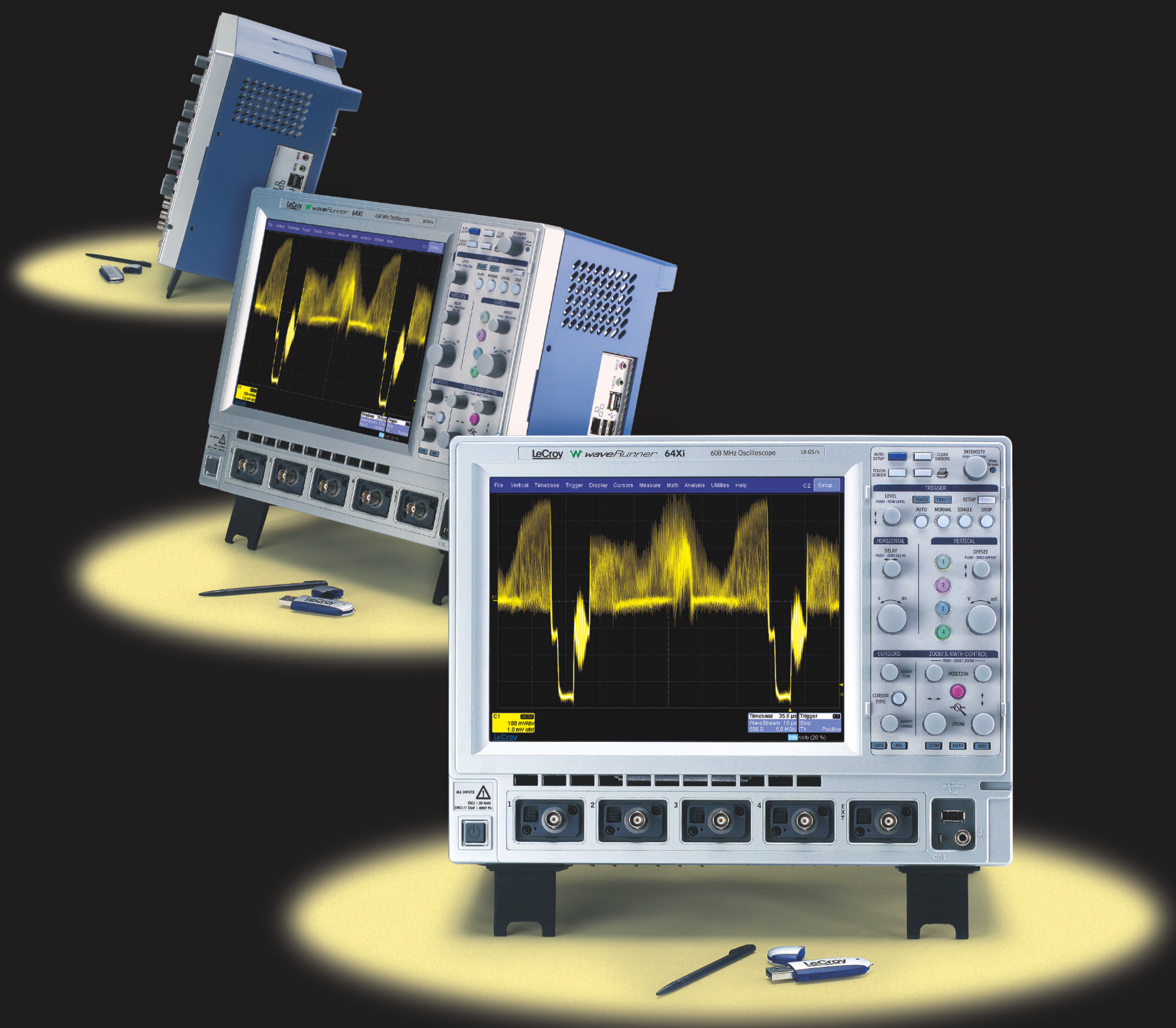

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Virtual-current mode: current-mode control without the noise

THIS NEW DC/DC-SWITCHING-REGULATOR DESIGN APPROACH COMBINES THE BEST FEATURES OF CURRENT- AND VOLTAGE-MODE CONTROL.

The two most common forms of control in dc/dc switching power converters are CM (current-mode) and VM (voltage-mode) control. Each method has its own advantages and disadvantages. CM control provides the ease of loop compensation and inherent line feedforward, which makes this method a favorite among designers. VM control is more immune to noise. This characteristic is important in large-step-down-ratio applications in which the switch has a short on-time that is susceptible to noise pickup. The ideal approach that has been eluding designers is a practical CM-controlled regulator without noise-susceptibility challenges.

Figure 1 shows a buck regulator using VM control. The system monitors the output voltage and compares it with a reference voltage. The resulting error signal and a modulating ramp form a PWM (pulse-width modulator), which controls the buck switch. In each cycle, the clock turns on the buck switch, which the PWM comparator then turns off. A first-order approximation for the buck-switch duty cycle, D, is $D=V_{OUT}/V_{IN}$. The modulating ramp in VM control is a dedicated sawtooth-ramp-oscillator circuit. The modulation is more stable and less noise-sensitive if you use a fixed sawtooth ramp, because the ramp amplitude is fairly large—often, 2 to 3V peak. The disadvantages of VM control are difficulties in designing the loop compensation and the inherent lack of feedforward.

Figure 2 shows a buck regulator using CM control. The system monitors the output voltage, compares it with a reference, and applies the resulting error signal to the PWM. The origin of the modulating ramp is an area in which VM and CM control differ. The modulating ramp in CM control is a signal proportional to the buck-switch current. When you turn on the buck switch, the inductor current flows through it. During this time, the inductor current has a positive slope of $(V_{IN}-V_{OUT})/L$. An accurate fast measurement of the buck-switch current is necessary to create the modulating-ramp signal. The main disadvantage of CM control is the difficulty of creating the buck-switch-current signal.

ALMOST IMPOSSIBLE

Propagation delays and noise susceptibility make it almost impossible to use CM control for high-input-voltage, large-step-down applications that require small on-times. For example, a buck regulator with an input voltage of 66V and an output voltage of 3.3V requires a buck-switch duty cycle of 5%. If the clock frequency is 300 kHz with a period of 3.3 μsec, the required on-time for the buck switch is only 166 nsec. Therefore, during each cycle, the buck switch must turn on, the ramping buck-switch current must be measured and level-shifted, the PWM comparator must change state, and the buck switch must turn off—all within 166 nsec.

The buck regulator's modulating switch is floating; that is, none of the switch terminals connect to ground. The buck switch's source terminal is at the input potential, V_{IN}, when the switch is on and is at approximately −1V when the switch is off. Measuring the switch current is challenging. The measurement choices are to place a shunt resistor or a current-sense transformer in the buck-switch drain, to make a measurement across the buck switch's on-resistance, or to use a current-mirror circuit coupled to the buck switch. Each of these methods requires a level shift to transpose the measured signal down to the ground reference for appli-

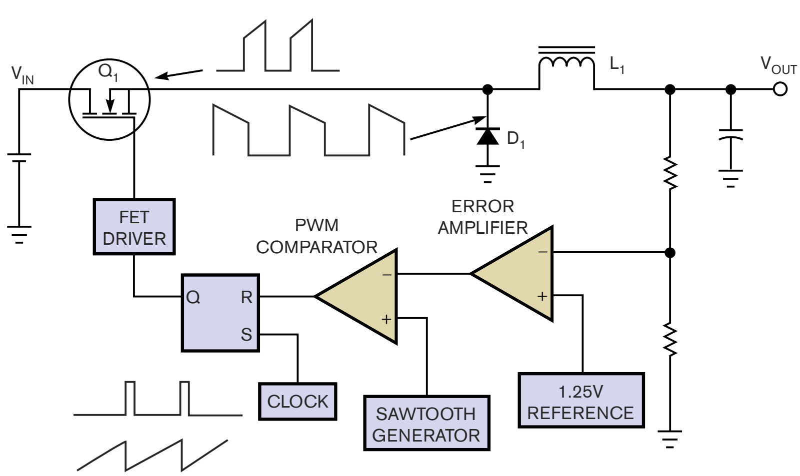


Figure 1 In this voltage-mode buck regulator, the error signal and a modulating ramp form a pulse-width modulator, which controls the buck switch.

cation to the PWM comparator. Even with the best design practices, the level-shift circuit inserts a significant propagation delay. Higher input-voltage applications exaggerate this delay.

Even if you can design a fast, accurate current-measurement circuit and a level shifter, numerous challenges remain. When the buck switch turns on, the free-wheel diode, D_1, turns off. To turn off the diode, an appreciable amount of reverse charge flows during the recovery time in the form of a reverse-recovery current. This diode's reverse current also flows through the buck switch, causing a leading-edge current spike and an extended ringing period. This spike can cause the PWM comparator to trip prematurely and cause erratic operation. The most common approach to solving this problem is to add filtering or leading-edge blanking to the current-sense signal. This blanking and filtering further limit the minimum controllable buck-switch on-time.

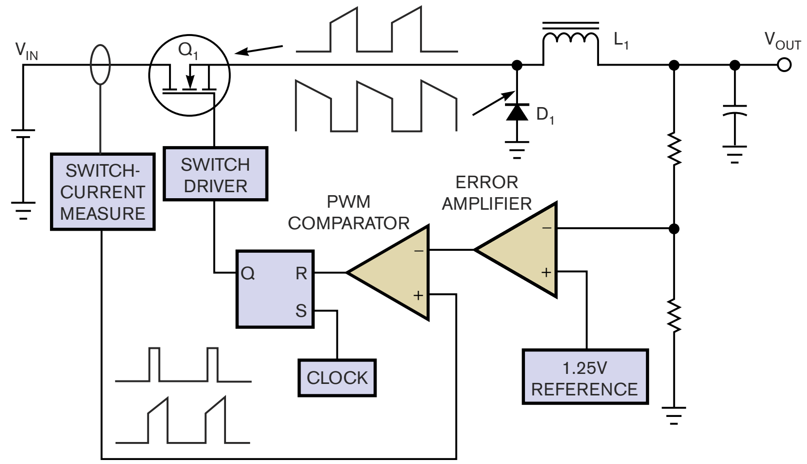


Figure 2 The principal difference between this current-mode regulator and the voltage-mode circuit is in the source of the modulating ramp. In this circuit, the ramp voltage is proportional to the buck-switch voltage.

EMULATED CURRENT-SENSE SIGNAL

An alternative approach to measuring the actual current flowing through the buck switch is to develop a signal that emulates the buck-switch current without making an actual current measurement. The three main current waveforms in a buck regulator are the buck-switch current, the free-wheel-diode current, and the inductor current. The buck-switch and the diode currents sum to form the inductor current (**Figure 3**). Taking a closer look at the characteristics of the buck-switch-current waveform, you can see that the signal breaks down into two parts—a base pedestal and a ramp. The pedestal represents the minimum inductor-current value over the switching cycle. The inductor current is at its minimum the instant the free-wheel diode turns off, just as the buck switch turns on. In each switching cycle, the buck switch and the diode have the same minimum-current value, which occurs when the inductor current is at its lowest value. Taking a sample-and-hold measurement of the free-wheel-diode current just before the buck switch turns on can capture the pedestal-level information.

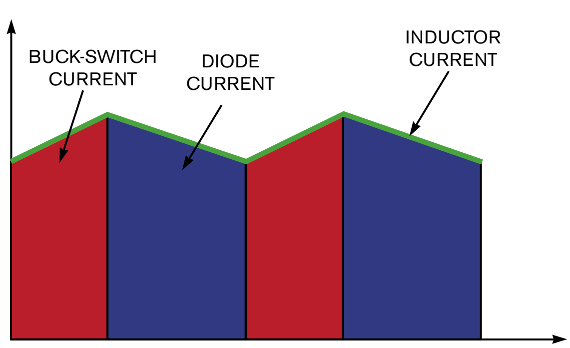


Figure 3 The three main current waveforms in a buck regulator are the buck-switch current, the free-wheel-diode current, and the inductor current. The buck-switch and the diode currents sum to form the inductor current.

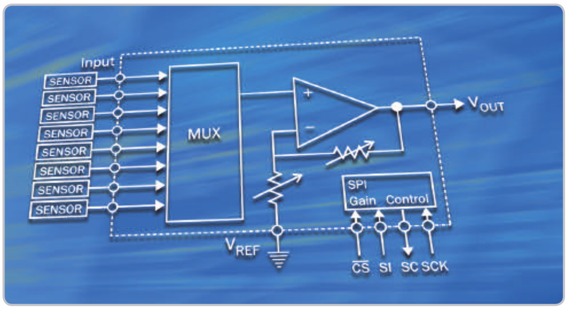
The other part of the buck-switch-current signal is the ramp. When the buck switch turns on, the voltage across the output inductor is the difference between the input, V_{IN}, and the output, V_{OUT}, voltages. This voltage difference forces a positively ramping current through the inductor and the buck switch. The ramping current's slope is equal to: $di/dt=(V_{IN}-V_{OUT})/L$. A voltage-controlled current source, I_{RAMP}, and a ramp capacitor, C_{RAMP}, can create an equivalent signal.

The slope of the rising voltage across a capacitor, which current source I_{RAMP} drives, equals $dv/dt=I_{RAMP}/C_{RAMP}$. If the difference between the input and the output voltages controls the current source, the slope of the capacitor-ramp voltage equals $dv/dt=K\times(V_{IN}-V_{OUT})/C_{RAMP}$, where K is the current-source scale factor.

Figure 4 shows a practical controller that emulates the buck-switch-current signal and uses that signal for CM control. The top portion of the diagram shows the normal buck-regulator power-switching components. The free-wheel diode's anode connects to ground through the controller. A small-value current-sense resistor and amplifier measure the diode current. The combined sense-resistor/amplifier scale factor is 0.5V/A. A sample-and-hold circuit captures the diode-current minimum value just before the buck switch turns on. Sampling each cycle, this circuit captures the pedestal portion of the emulated buck-switch current-sense signal.

CONTROLLED CURRENT SOURCE

The controller also senses the input and output voltages. The difference between these two signals controls a current source. This current source charges the external ramp capacitor. In each cycle, when the buck switch turns on, the capacitor voltage rises linearly. When the buck switch turns off, the capacitor rapidly discharges and shunts the current source to ground. The current-source scale factor is: $I_{RAMP}=(5\times10^{-6}\times(V_{IN}-V_{OUT}))$. The desired overall scale factor for the emulated ramp signal is



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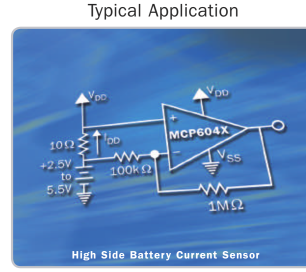

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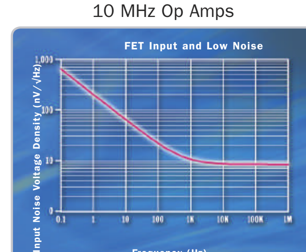

0.5V/A. For proper operation, set the ramp-capacitor value proportional to the output-inductor value. A good starting point is to select $C_{RAMP}=L\times10^{-5}$, where the units of L are henries and those of C_{RAMP} are farads. Using this value scales the capacitor-ramp voltage to half the output-inductor current, consistent with the sample-and-hold-circuit scale factor. The derivation is as follows. Set inductor slope equal to the capacitor slope:

$$\frac{di}{dt}=\frac{dv}{dt}.$$

$$\frac{(V_{IN}-V_{OUT})}{L}=\frac{5\times10^{-6}\times(V_{IN}-V_{OUT})}{C_{RAMP}}.$$

$$C_{RAMP}=L\times5\times10^{-6}.$$

For a scale factor of 0.5V/A, the value of C_{RAMP} is $L\times10^{-5}$.

The final step in generating the emulated buck-switch-current signal is to sum the pedestal information (from the sample and hold) with the ramp-capacitor-voltage signal. **Figure 5** shows the final summed waveform. This signal is now ready for use in the PWM comparator, as well as in the current-limit comparator.

For applications that operate with duty cycles greater than 50%, CM-controlled circuits are subject to subharmonic oscillation. By adding another fixed-slope voltage-ramp signal (slope compensation) to the current-sense signal, you can avoid this oscillation. Referring to the ramp-generator circuit, an additional, fixed, 25-µA offset current provides some fixed slope to the capacitor-voltage-ramp signal. Very-high-duty-cycle applications may require additional slope. For these applications, you can decrease the ramp-capacitor value to increase the ramp slope and prevent subharmonic oscillation.

You can accomplish output-overload protection by either clamping the error signal or providing a dedicated current-limit comparator. This type of overload protection, cycle-by-cycle current limiting, yields an almost-immediate response, which protects the buck switch. Virtual CM has an added benefit of capturing the pedestal information before the buck switch turns on. During extreme overloads at high input voltage, the buck switch skips cycles, preventing possible runaway current conditions.

A CM-controlled regulator's control-to-output transfer function has a single-pole characteristic despite an output stage that

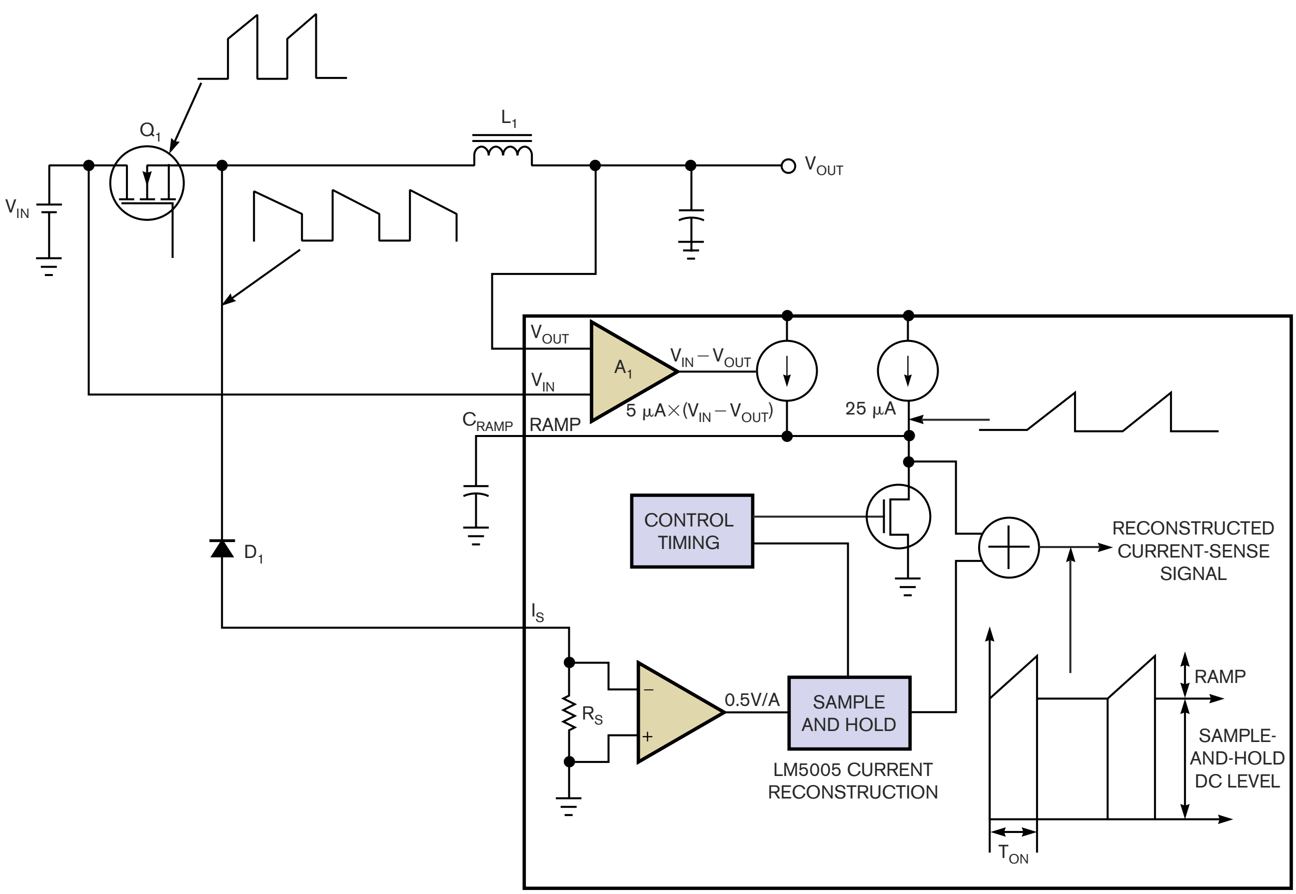

Figure 4 This practical controller overcomes current-mode regulators' noise susceptibility by emulating the buck-switch-current signal and using the emulated signal for current-mode control.

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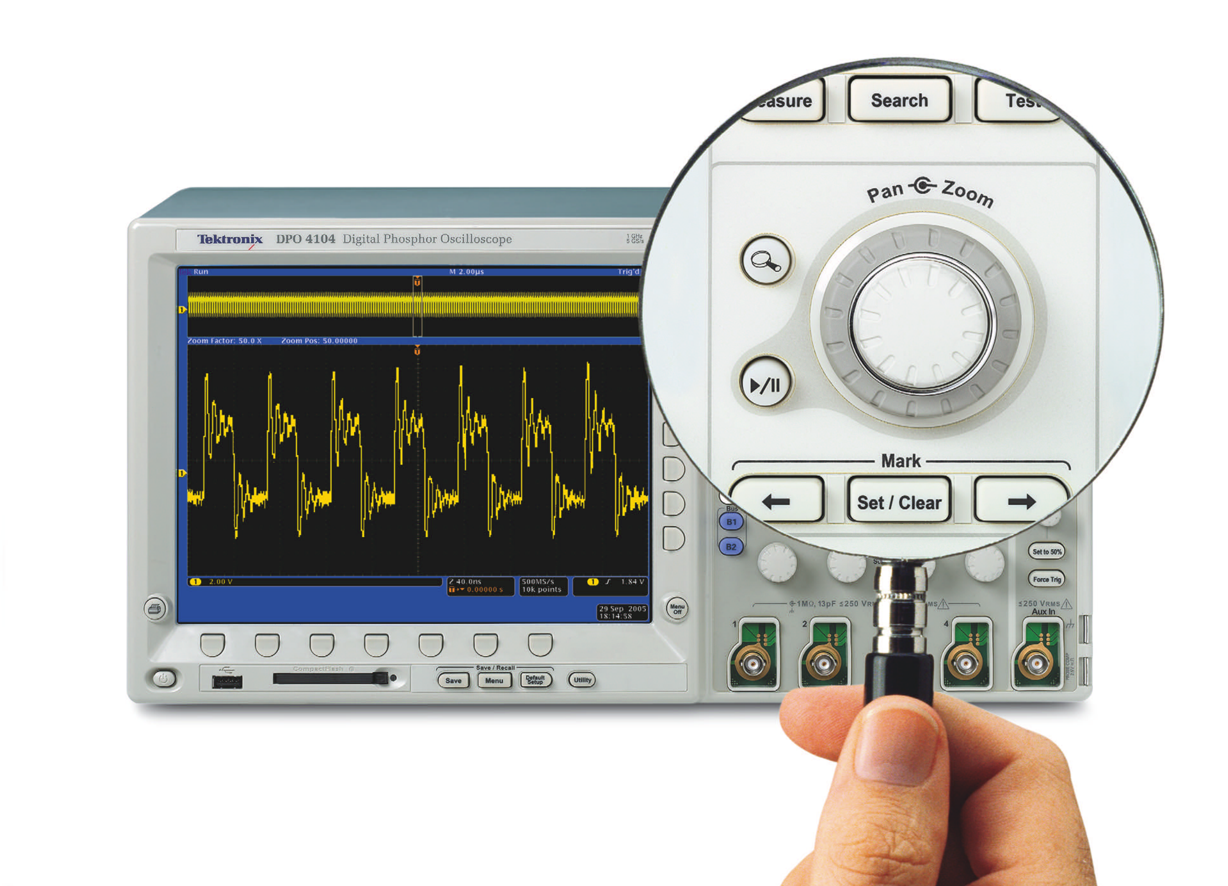

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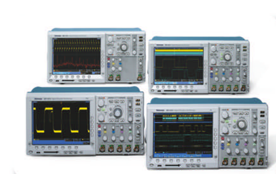

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comprises two main elements, L and C. The characteristic has only one pole because there are two control loops: a voltage loop, which keeps the output voltage constant, and an inner current loop. The current loop monitors and controls the inductor current, forcing the inductor to act as a constant-current source programmed by the voltage loop. Because the inductor behaves as a constant-current source, the control-to-output transfer function has only one pole, which the output capacitor, C_O, and load resistance, R_L, establish. This pole occurs at a frequency of $f_P=1/(2\pi C_O R_L)$. There is also a zero at $f_Z=1/(2\pi C_O R_{ESR})$ because of the output capacitor's ESR (equivalent series resistance). Hence, the required error-amplifier compensation comprises an integrator for good line/load regulation and low output impedance; a zero to cancel the load pole; and if necessary, a pole to cancel the ESR zero.

During light loading, the inductor current decays to zero for part of the cycle. This light-load mode is referred to as discontinuous operation. An advantage of CM control is that no stability problems exist in the discontinuous-conduction mode because the regulator remains a single-pole, single-zero system under both continuous and discontinuous operating modes. Another advantage of CM control is inherent feedforward, because the inductor-current ramp is a function of the input voltage. Any input-voltage change immediately changes the modulating-ramp slope and corrects the duty cycle without the need for the regulation loop to react—that is, to feed forward.

TEST RESULTS

A buck regulator with an input-voltage range of 7 to 75V, an output voltage of 5V, and a 2.5A current capability demonstrates the emulated-CM-control operation (**Figure 6**). The 300-kHz operating frequency represents a good trade-off between efficiency and component size. A conventional Type II pole-zero compensation network commonly used for CM control accomplishes loop compensation. The resulting loop-bandwidth-crossover frequency is 20 kHz. At 75V input, the step-down ratio is 15-to-1, requiring a buck-switch on-time of 222 nsec in continuous-mode operation. Measured, stable on-times of approximately 100 nsec occur during discontinuous-mode operation.

Emulated CM control applies not only to buck regulators, but also to isolated buck-regulator-based topologies, such as forward, half-bridge, and full-bridge. EDN

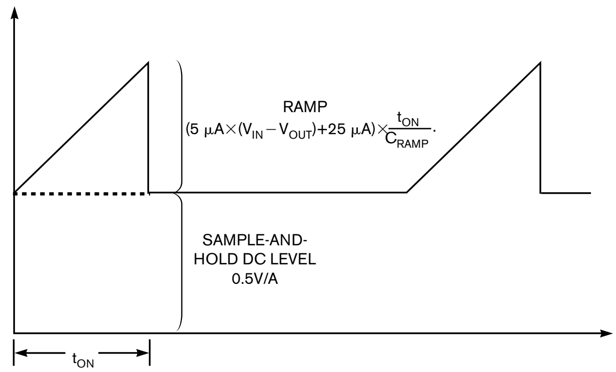

Figure 5 The final summed waveform is ready for use in the pulse-width-modulator comparator, as well as in the current-limit comparator.

AUTHOR'S BIOGRAPHY

Robert Bell is the applications-engineering manager for National Semiconductor's Design Center (Phoenix), where he has worked for four years. The center's products include next-generation PWM power controllers, gate drivers, and hot-swap and load-share controllers. Before joining National Semiconductor, Bell designed power converters for military and space applications. In his spare time, he enjoys hiking, camping, tennis, and travel.

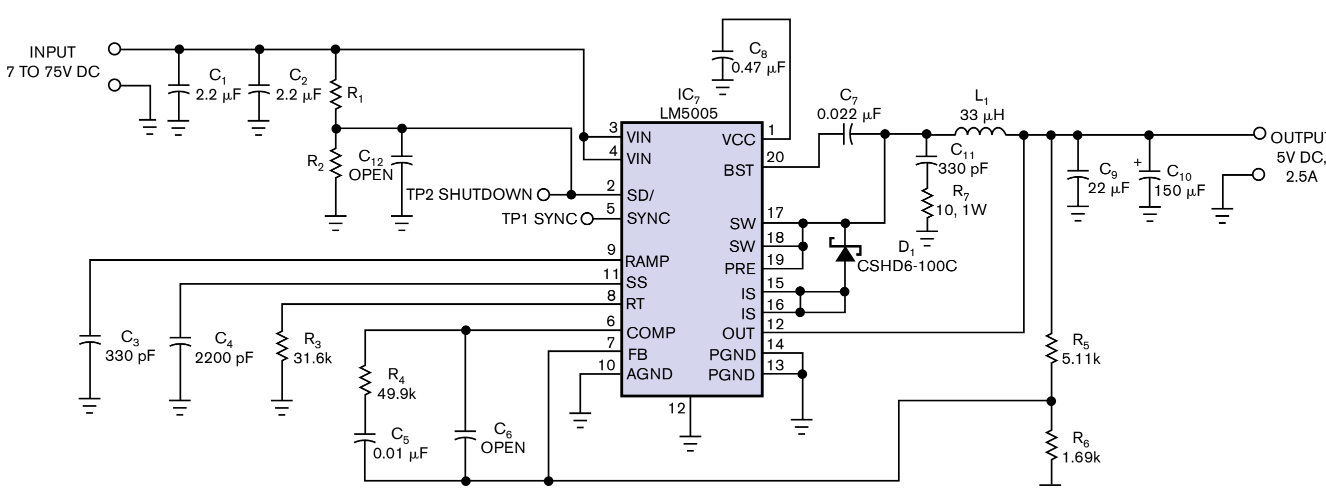

Figure 6 During discontinuous-mode operation, this regulator achieves stable on-times as low as approximately 100 nsec.

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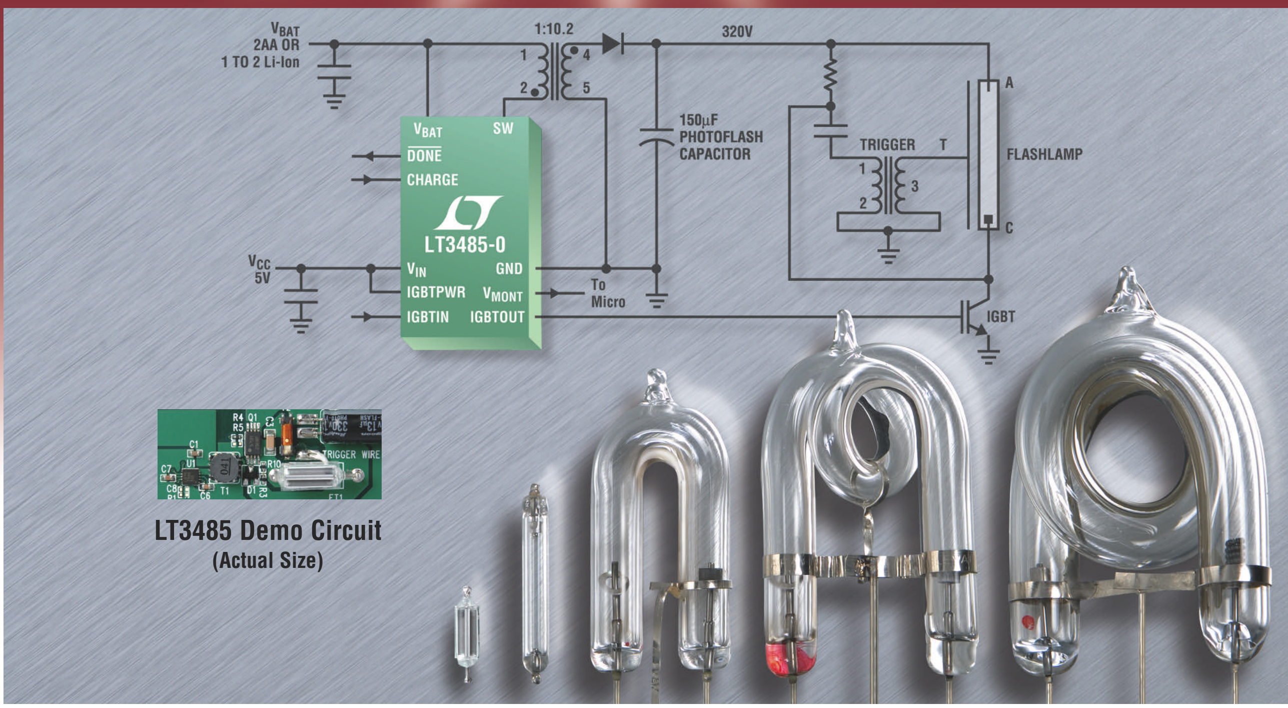

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Lowpass, 30-kHz Bessel filter offers high performance for audio applications

Troy Murphy, Analog Devices, San Jose, CA

Thanks to its property of applying an equal amount of delay to all frequencies below its cutoff frequency, the Bessel linear-phase filter sees service in audio applications in which it's necessary to remove out-of-band noise without degrading the phase relationships of a multifrequency in-band signal. In addition, the Bessel filter's fast step response and freedom from overshoot or ringing make it an excellent choice as a smoothing filter for an audio DAC's output or as an antialiasing filter for an audio ADC's input. Bessel filters are also useful for analyzing the outputs of Class D amplifiers and for eliminating switching noise in other applications to improve accuracy of distortion and oscilloscope-waveform measurements.

Although the Bessel filter provides flat magnitude and linear-phase—that is, uniform group-delay—responses within its passband, it has worse selectivity than Butterworth or Chebyshev filters of the same order, or number of poles. Thus, to achieve a given level of stopband attenuation, you need to design a higher order Bessel filter, which, in turn, requires careful selection of amplifiers and components to achieve the lowest levels of noise and distortion.

Figure 1 shows a schematic for a high-performance, eighth-order, 30-kHz, lowpass Bessel filter. This design uses standard values for 1%-tolerance resistors and 5%-tolerance ceramic capacitors. As an alternative, you can use 10%-tolerance capacitors at the expense of increased group-delay variance within the passband. For best results, use temperature-stable capacitors.

In this application, the filter processes audio signals that swing above and below ground, and its amplifiers draw power from positive and negative ±2.5V supplies. Rail-to-rail output capability helps achieve maximum output-voltage swing at these low supply voltages. To achieve a high SNR in high-quality audio service, the amplifiers must exhibit unity-gain stability and low inherent noise. For example, Analog Devices' AD8656 low-noise, precision-CMOS dual op amp meets all of these requirements.

Connecting the amplifiers as inverting-gain stages maintains constant input-common-mode voltage and helps minimize distortion. Using less-than-1-kΩ resistors throughout the circuit reduces the resistors' thermal-noise contributions. Each AD8656 amplifier contributes less than 3 $nV/\sqrt{Hz}$ of noise across a 30-kHz bandwidth, and the total noise over a 30-kHz bandwidth measures less than 3.5 μV rms. For a 1V-rms input signal, the circuit yields an SNR of better than 109 dB, and, for a 1-kHz, 1V-rms input signal, the circuit yields a THD+N (total-harmonic-distortion-plus-noise) factor of better than 0.0006%.

Figure 2 shows the filter's measured magnitude response for a 1V-rms input signal. The filter's passband gain of 0 dB is flat within 1.2 dB for frequencies as

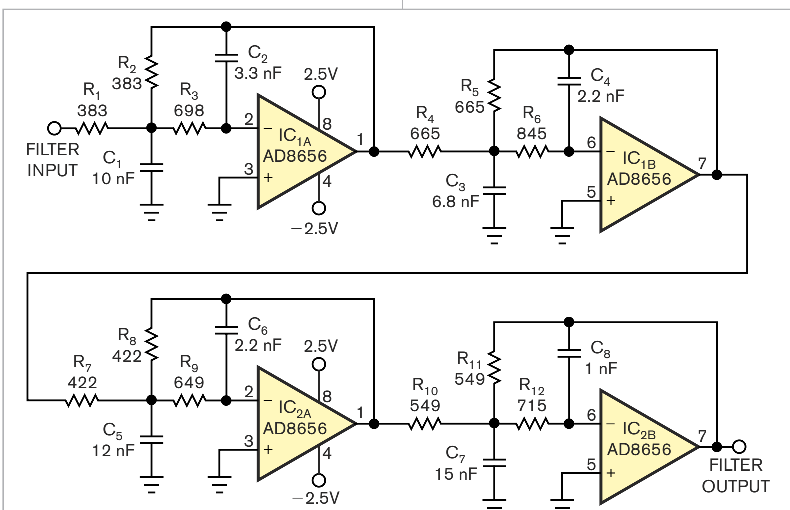

Figure 1 Two dual op amps and a handful of passive parts implement a high-performance, eighth-order, 30-kHz, lowpass Bessel filter.

DIs Inside

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high as 20 kHz. With its −3-dB point at 30 kHz, an eighth-order Bessel presents a theoretical attenuation of −110 dB at 300 kHz, decreasing at −160 dB/decade at higher frequencies. This characteristic provides sufficient attenuation of repetitive noise that switched-mode power supplies and other sources induce, which typically occurs at frequencies of 300 kHz and higher.

Figure 3 illustrates the filter's phase shift and its group delay, which remains relatively constant at roughly 17 μsec, even for frequencies as high as 40 kHz. Note the linear scale on **Figure 3**'s frequency axis, which clearly illustrates the filter's linear-phase behavior within the passband. The following **equation** defines group delay as the negative partial derivative of phase shift with respect to frequency:

$$\text{Group delay} = -\delta\phi/\delta f.$$

At dc, resistor R_1 sets the filter's input resistance at 383Ω. If your application requires higher input impedance, you can insert a unity-gain buffer ahead of the filter at the expense of increased distortion and noise. For applications that require operation from ±15V power supplies, replace the AD8656 with a higher voltage amplifier, such as Analog Devices' AD8672 low-distortion, low-noise (3.8-nV/$\sqrt{\text{Hz}}$), dual operational amplifier. EDN

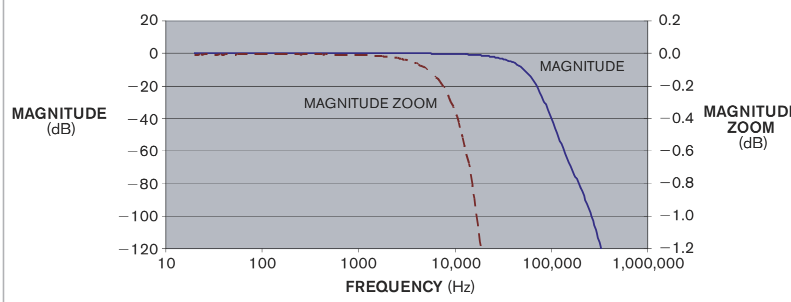

Figure 2 The measured amplitude-versus-frequency response of the circuit in Figure 1 shows a change of scale on the right vertical axis.

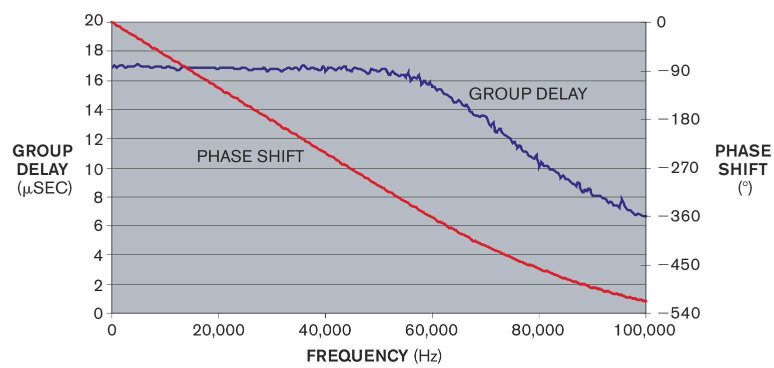

Figure 3 Measured within the passband of dc to 30 kHz, the Bessel filter's phase-shift and group-delay characteristics display excellent uniformity and linearity.

Use a PWM fan controller in an EMI-susceptible circuit

Dimitri Danyuk, Niles Audio Corp

Microchip Technology (www.microchip.com) offers a family of cooling-fan speed controllers that operate in PWM mode for use with brushless dc fans (**Reference 1**). To control fan speed using the PWM waveform's duty cycle, you can use either an external NTC (negative-temperature-coefficient) thermistor or one of Microchip's PIC microcontrollers and its SMBus serial-data bus. **Figure 1** illustrates a typical application that the data sheet describes for the TC664 and TC665 controllers (**Reference 2**). Using a frequency-control capacitor, C_F, with a value of 1 μF, fan-controller IC_1 generates a PWM pulse train with a nominal frequency of 30 Hz and a temperature- or command-dependent duty cycle that varies from 30 to 100%.

Although using the controller in PWM mode reduces power dissipation in transistor Q_A, which drives the fan, the 100-mA, square-wave motor-drive current can cause unwanted interference in a nearby high-sensitivity audio circuit. The circuit in **Figure 2** solves the problem. An additional driver transistor, Q_1, and an RC network comprising C_3 and R_3 form a simple PWM-to-linear converter. You can also use another PWM-to-linear-conversion circuit, such as an integrator based on an operational amplifier.

Figure 3 shows a graph of the dc voltage at Q_2's collector versus IC_1's PWM

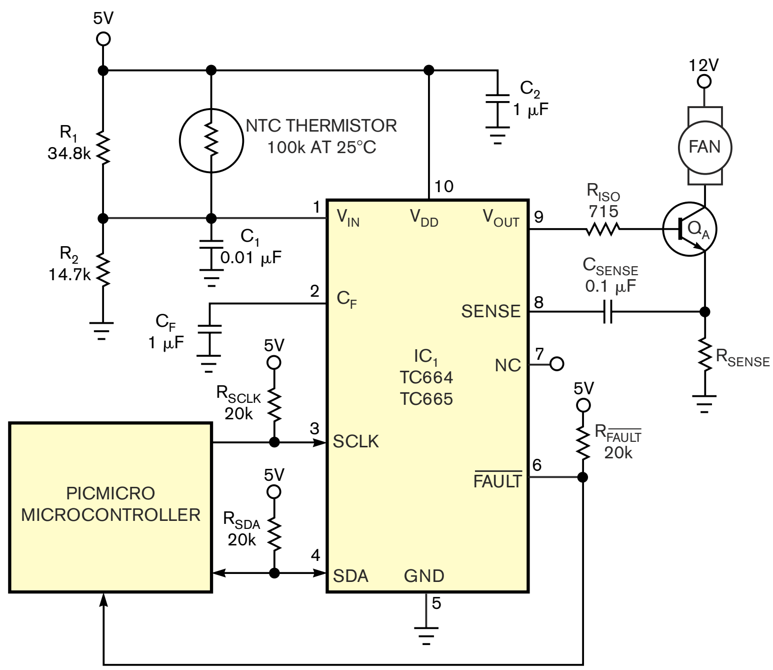

Figure 1 In a typical application, fan-controller IC_1 and transistor Q_A apply pulse-width-modulated current to vary a fan's speed as a function of temperature.

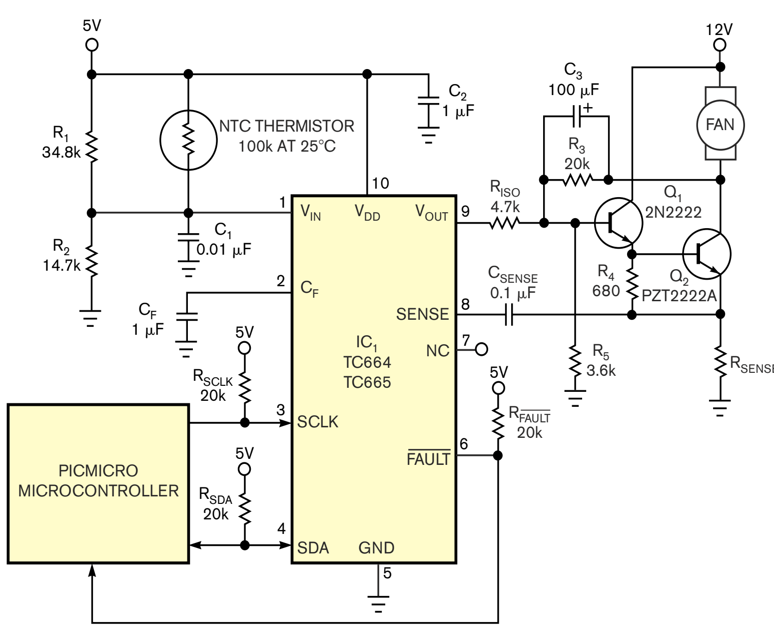

Figure 2 To minimize the effects of high-frequency noise on sensitive analog circuits, you can convert the high-current PWM waveform applied to the fan to a continuous analog voltage.

drive-output waveform's duty cycle. The voltage applied to the fan corresponds to the difference between Q_2's collector voltage and the 12V supply voltage. Even though a steady voltage appears across the fan, current pulses that the fan motor's commutation produces still develop a voltage across current-sense resistor R_{SENSE} that connect to Q_2's emitter, and all of IC_1's protective and advisory features remain available.

The listed component values are valid for a 100-mA, 12V, brushless fan. Use a general-purpose NPN transistor such as the 2N2222 for driver-transistor Q_1 and an NPN transistor, such as Fairchild Semiconductor's PZT2222A, that can dissipate one-third of the fan's maximum power consumption for Q_2. Note that you can vary the PWM's nominal frequency over a range of 15 to 35 Hz by altering the value of C_F. **EDN**

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1 "Fan Speed Controller and Fan Fault Detector Family," Microchip Technology Inc, 2002, http://ww1.microchip.com/downloads/en/DeviceDoc/21604c.pdf.

2 SMBus PWM Fan Speed Controllers with Fan Fault Detection, Microchip Technology Inc, 2003, http://ww1.microchip.com/downloads/en/DeviceDoc/21737a.pdf.

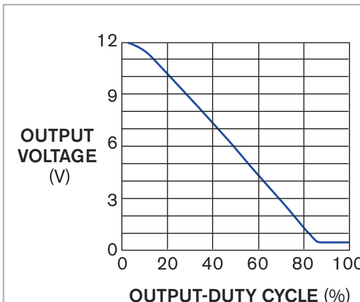

Figure 3 Output voltage at Q_2's collector shows a linear relationship versus the controller's pulse-width-modulated output-duty cycle. (The pulse width increases as the temperature increases.) The fan's operating voltage corresponds to the difference between Q_2's output voltage and the 12V supply rail.

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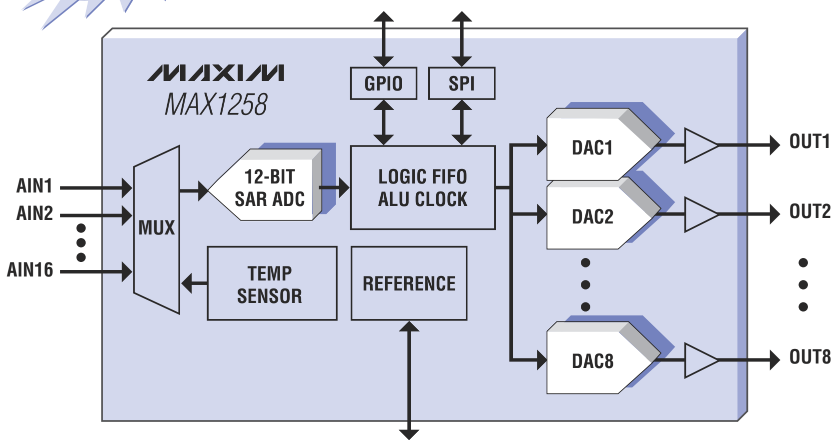

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MAX1222/1022	+4.75 to +5.25	12	8	0	4.096	10/12	1	36-QFN
MAX1221/1021	+2.7 to +3.6	8	8	8	2.048	10/12	1	36-QFN
MAX1220/1020	+4.75 to +5.25	8	8	4	4.096	10/12	1	36-QFN
MAX1343/1043	+2.7 to +3.6	8	4	4	2.048	10/12	1	36-QFN
MAX1342/1042	+4.75 to +5.25	8	4	4	4.096	10/12	1	36-QFN
MAX1341/1041	+2.7 to +3.6	8	4	0	2.048	10/12	1	36-QFN
MAX1340/1040	+4.75 to +5.25	8	4	0	4.096	10/12	1	36-QFN
MAX1349/1049	+2.7 to +3.6	4	4	4	2.048	10/12	1	36-QFN
MAX1348/1048	+4.75 to +5.25	4	4	4	4.096	10/12	1	36-QFN
MAX1347/1047	+2.7 to +3.6	4	4	0	2.048	10/12	1	36-QFN
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PC's parallel port and a PLD host multiple stepper motors and switches

Eduardo Pérez-Lobato, Universidad de Antofagasta, Antofagasta, Chile

Robotic applications frequently include multiple stepper motors and switches. The stepper motors produce motion in several directions, and the switches identify home positions and detect proximity to obstacles. This Design Idea describes the development and implementation of a PLD (programmable-logic-device)-based interface that can connect a PC's parallel port to as many as eight switches and four stepper motors (**Figure 1**). This interface design serves many applications, and using IC_1, a 22V10 PLD, to minimize the circuit's component count reduces complexity, weight, and overall dimensions. Drivers IC_3 through IC_6 for the stepper motors comprise three L293 quad half-H-bridge ICs (**Figure 2**).

Each rotation of the two-winding stepper motors in this design requires a sequence of four mechanical steps that you produce by applying a pair of 7V, 500-mA, 120-msec-long pulses to the motor's windings (**Figure 3**). To make a stepper motor rotate either CW (clockwise) or CCW (counterclockwise), you apply either of two pulse sequences (**tables 1** and **2**).

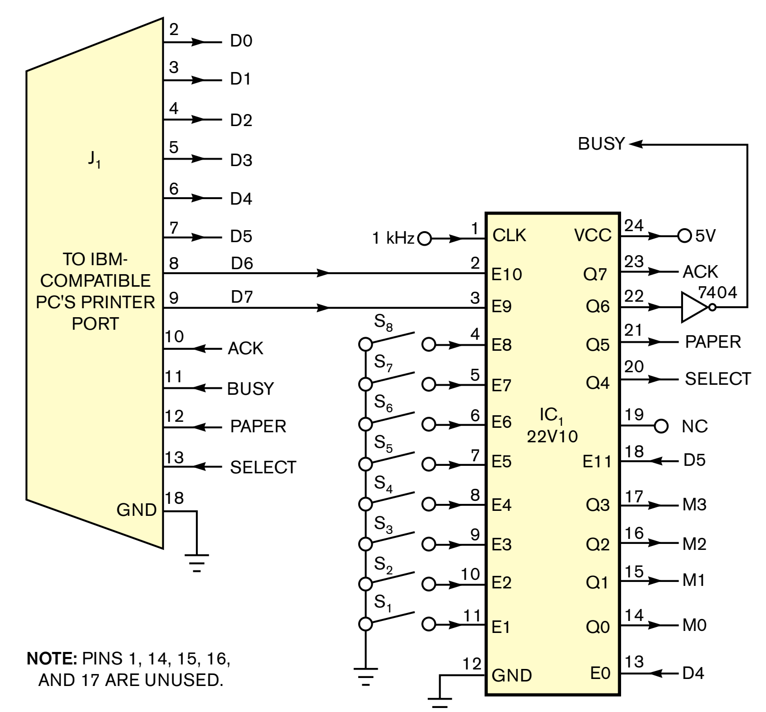

Figure 1 A programmable-logic device, IC_1, and a few additional components allow an IBM-compatible PC's parallel printer port to drive as many as four external stepper motors and to sense the states of as many as eight range-of-motion limit switches.

The following sections specify the functions of the input and output registers' bits that control the parallel-port interface and the PLD. The PLD output-register bits are 7, 6, 5, 4, 3, 2, and 1. Q7 signals the PC that one or more switches are active. Bit 0 means that a switch is active; bit 1 means that no switches are active. With Q6, Q5, and Q4, the BSS (buffered-status switch) tells the PC which of n switches is active: 000=S_1, 100=S_5, 001=S_2, 101=S_6, 010=S_3, 110=S_7, 011=S_4, and 111=S_8. For Q3, Q2, Q1, and Q0, the PLD's outputs enable one of the four motor-driver ICs to drive its associated stepper motor, with 1000=M_3, 0010=M_1, 0100=M_2, and 0001=M_0.

The PLD input register's bits are E11, E10, E9, and E0. For E11, the host PC controls the PLD, 0 disables the PLD, and 1 enables the PLD. For E10 and E9, the PLD reads these lines to determine which of the four motors in **Figure 2** receives drive pulses: 00 for Motor 0, 10 for Motor 2, 01 for Motor 1, and 11 for Motor 3. For bit E0, the PLD reads this bit to determine what to do with the BSS settings: 0=hold, and 1=clear. For E8 through E1, the PLD reads the status of one switch and stores it in the BSS register:

00000001=S_1, 00010000=S_5,
00000010=S_2, 00100000=S_6,
00000100=S_3, 01000000=S_7,
00001000=S_4, 10000000=S_8.

The PLD ignores any unlisted bits.

For the parallel-port output register, address 888_{10}, D7, and D6, the PC tells

TABLE 1 CLOCKWISE-ROTATION SEQUENCE

Step	A	B	C	D
0	1	1	0	0
1	0	1	1	0
2	0	0	1	1
3	1	0	0	1

TABLE 2 COUNTERCLOCKWISE-ROTATION SEQUENCE

Step	A	B	C	D
0	1	0	0	1
1	0	0	1	1
2	0	1	1	0
3	1	1	0	0

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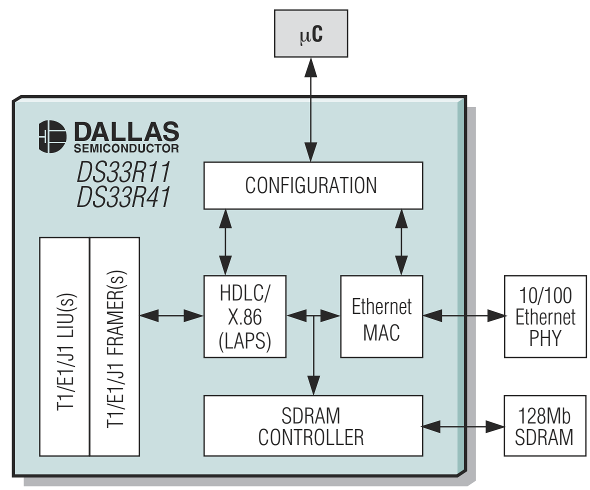

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the PLD which motor should run, with 00 for Motor 0, 10 for Motor 2, 01 for Motor 1, and 11 for Motor 3. For D5, the PC takes control of the PLD chip: 0 disables the PLD, and 1 enables the PLD. For D4, the PC commands the PLD to control the BSS register's contents, with 0 for hold and 1 for clear. For D3 through D0, the PC selects which pair of motor windings get energized: 1001=A and D, 1100=C and D, 0011=A and B, and 0110=C and B. Parallel-port input-register, address 888_{10}+1 indicates acknowledge, busy, paper, or select. The PC reads acknowledge to determine whether a switch is active: 0 means that any switch is active, and 1 means that no switch is active. The PC reads the busy, paper, or select register to determine which of the switches is active:

000=S_1, 011=S_4,
110=S_7, 001=S_2,
100=S_5, 111=S_8,
010=S_3, 101=S_6.

You can download **Listing 1** for this Design Idea from www.edn.com/060216di3. Note that the PC's portion of the software is written in Pascal, and the PLD's internal software is written in an emulated version of Basic. **EDN**

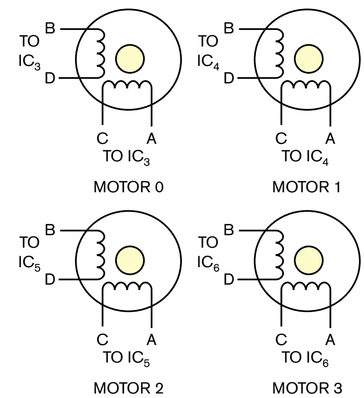

Figure 3 To control a stepper motor's direction of rotation, energize the windings as shown in tables 1 and 2.

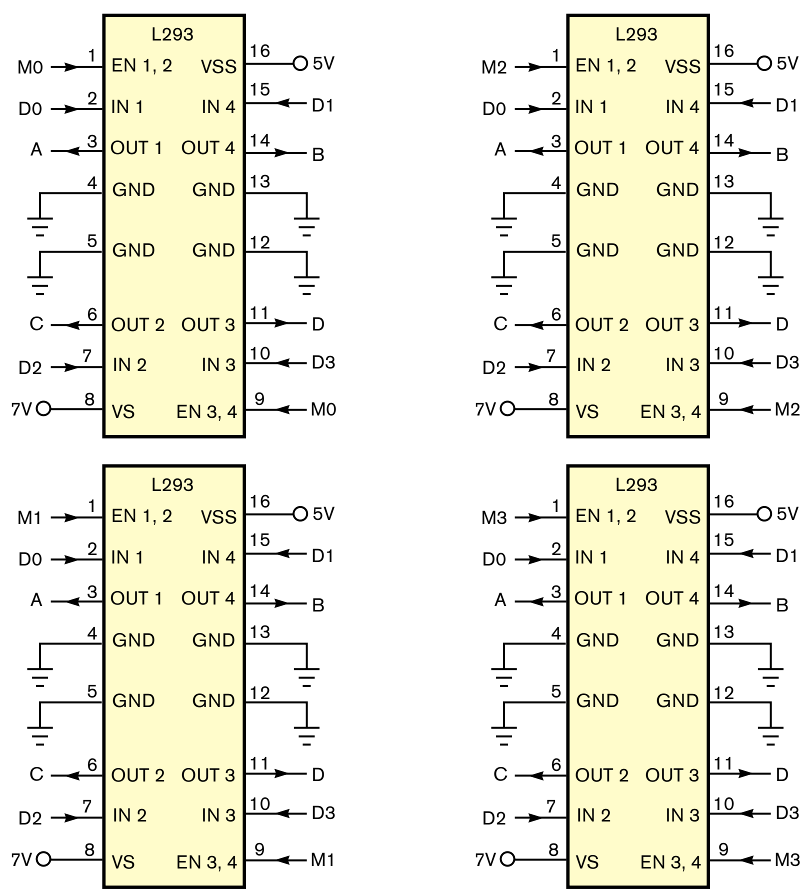

Figure 2 Each half-bridge-driver circuit, IC_3 through IC_6, controls a single two-winding stepper motor.

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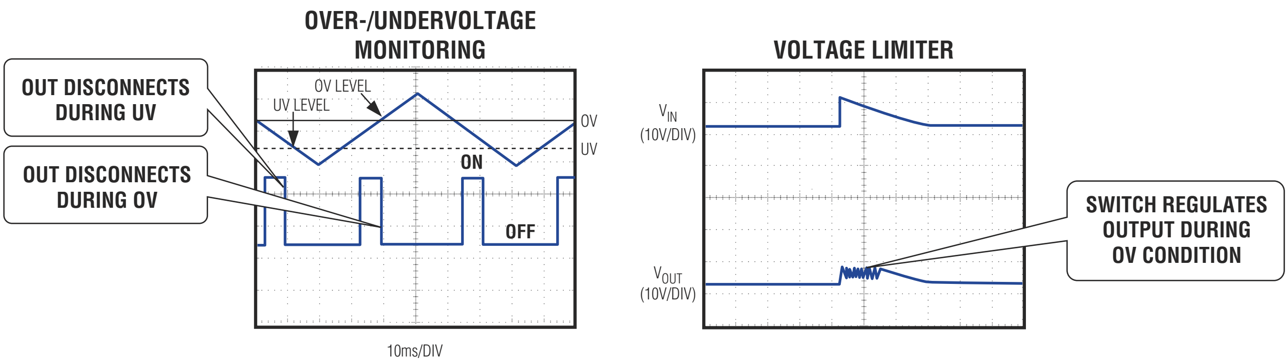

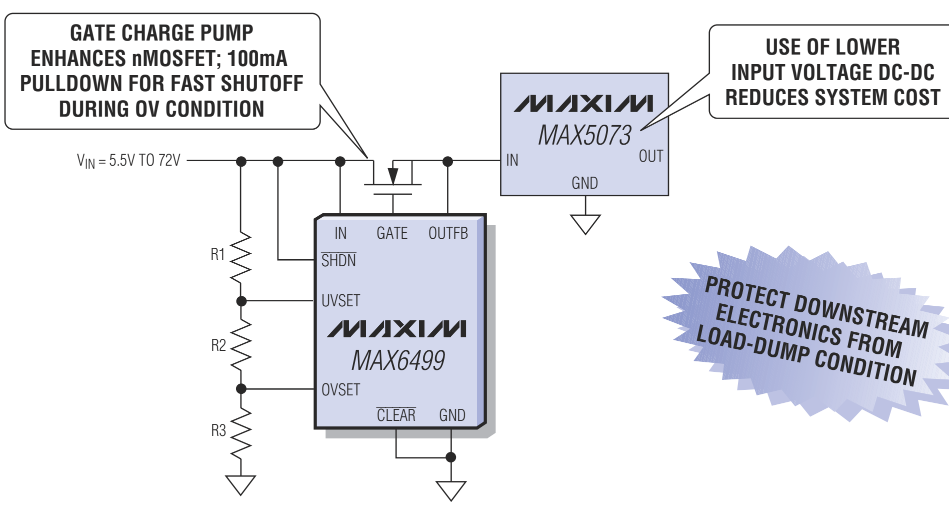

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MAX6495/MAX6496	Small, 6-lead OVP circuit
MAX6497/MAX6498/MAX6499	OV/UV monitoring, POK indicator, POK monitor, OV latch, window
MAX16010–MAX16014	Window monitoring, output-disable feature, p-channel comparator options

LINEAR TECHNOLOGY

DESIGN NOTES

Low EMI Synchronous DC/DC Step-Down Controllers Offer Programmable Output Tracking – Design Note 382

Lin Sheng

Introduction

The LTC®3808 synchronous DC/DC step-down controller packs numerous features required by the latest electronic devices into a low profile (0.75mm) 3mm × 4mm leadless DFN package or a leaded SSOP-16 package. Two similar parts, the LTC3809 and LTC3809-1, are even smaller, but less feature-rich versions of the LTC3808. The LTC3809 family is available in a 3mm × 3mm leadless DFN package or a 10-pin MSOP Exposed Pad package. All three parts can provide output voltages as low as 0.6V and output currents as high as 7A from a 2.75V to 9.8V input range, making them ideal devices for one or two lithium-ion cell inputs as well as distributed DC power systems.

The LTC3808 and LTC3809 also include important features for noise-sensitive applications, including a phase-locked loop (PLL) for frequency synchronization and spread spectrum frequency modulation to minimize generated electromagnetic interference (EMI). The adjustable operating frequency (300kHz to 750kHz) allows the use of small surface mount inductors and ceramic capacitors for compact power supply solutions.

Other features include:

- Low operating quiescent current to improve battery life and light load efficiency
- No R_{SENSE}™ current mode technology which senses the voltage across the main (top) power MOSFET to improve efficiency and reduce the size and cost of the solution
- Current mode control for excellent AC and DC line and load regulation
- Low dropout (100% duty cycle) for maximum energy extraction from a battery source
- Output overvoltage protection and short circuit current limit protection
- Adjustable or fixed built-in soft-start timer
- Output voltage ramp control and the ability to track other voltage sources (LTC3808 and LTC3809-1)
- PowerGood voltage monitor (LTC3808)

Table 1 compares the features of these three parts.

Table 1.

	START-UP CONTROL	SPREAD SPECTRUM	ADJUSTABLE FREQ/PLL	POWER GOOD
LTC3808	Internal External Tracking	Yes	Yes	Yes
LTC3809	Internal	Yes	Yes	No
LTC3809-1	Internal External Tracking	No	No	No

Three Choices for Start-Up Control

The start-up of V_{OUT} for the LTC3808 and LTC3809-1 is based on the three different connections to the TRACK/SS pin. A typical application is shown in Figure 2. When TRACK/SS is connected to V_{IN}, the start-up of V_{OUT} is controlled by the internal soft-start which ramps from 0V to (V_{FB}) in about 1ms. A second start up mode allows the 1ms soft-start time to increase or decrease by

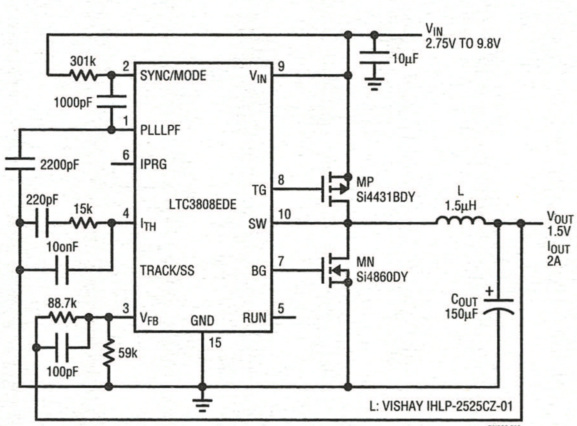

Figure 1. Synchronous Converter with Spread Spectrum Frequency Modulation

connecting an external capacitor C_{SS} between the TRACK/SS pin and ground. An internal 1µA current source and the value of C_{SS} control the ramp time of TRACK/SS from 0V to above 0.6V. In this case, the LTC3808 and LTC3809-1 regulate the VFB to the voltage at the TRACK/SS pin instead of the internal soft-start ramp. The third mode allows V_{OUT} of the LTC3808 and LTC3809-1 to track an external voltage, V_X, during start-up if a resistor divider from V_X is connected to the TRACK/SS pin. Figure 3 shows the start-up of V_{OUT} in these tracking modes for the circuit shown in Figure 2.

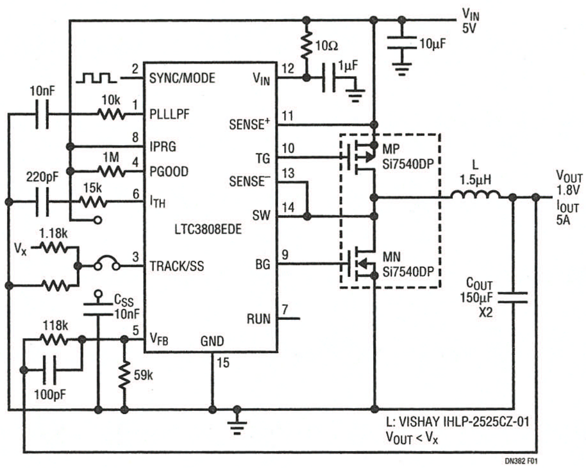

Figure 2. The LTC3808 Offers the Flexibility of Start-Up Control Based on the Three Different Connections on the TRACK/SS Pin

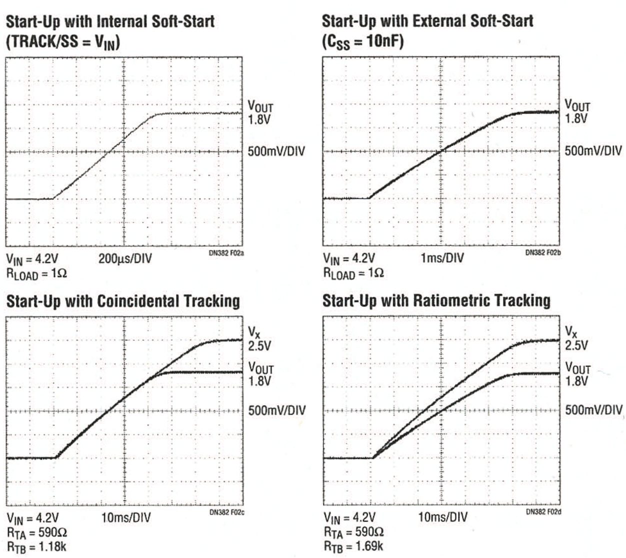

Figure 3. Start-Up Output Voltage Tracking Plots for Circuit in Figure 2

For simplicity, the LTC3809 only offers a 1ms internal soft-start.

Low EMI DC/DC Conversion

The LTC3808 and LTC3809 minimize the need for EMI shields and filters in applications such as navigation systems, wireless LANs, data acquisition boards and industrial and military radio devices by optionally spreading the nominal operating frequency (550kHz) over a range of frequencies between 460kHz and 635kHz. Spread spectrum frequency modulation is enabled by biasing the SYNC/MODE pin to a DC voltage between 1.35V and (V_{IN} – 0.5V). An internal 2.6µA pull-down current source at the SYNC/MODE pin can be used to set the DC voltage at this pin by tying a resistor with an appropriate value between SYNC/MODE and V_{IN}. Figure 1 shows the application circuit and Figure 4 shows the frequency spectral plots of the output (V_{OUT}) with and without spread spectrum modulation. Note the significant reduction in peak output noise (>20dBm) with spread spectrum enabled.

Conclusion

The LTC3808, LTC3809 and LTC3809-1 offer flexibility, high efficiency, low EMI and many other popular features in small thermally efficient packages. They offer excellent solutions for low voltage portable and distributed power systems that require a small footprint, high efficiency and low noise.

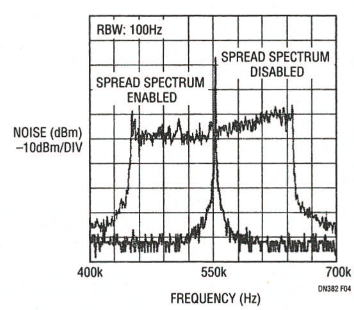

Figure 4. Comparison of the V_{OUT} Spectrum with and without Spread Spectrum Modulation Enabled

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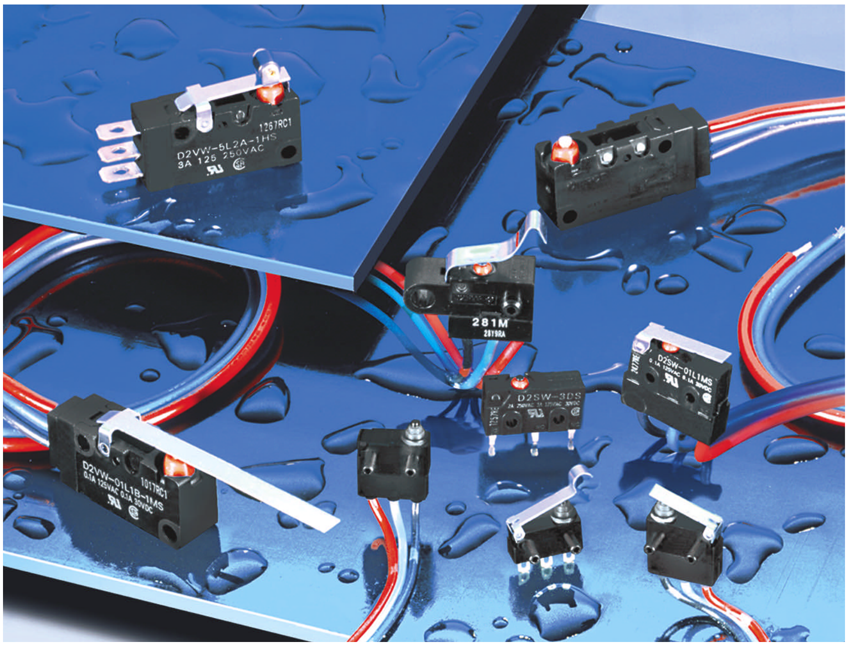
SWITCHES AND RELAYS



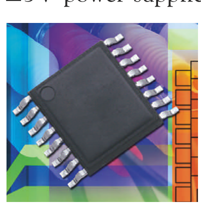
IP67-rated, sealed, snap-action switches suit transportation applications

Carrying an IP67 rating, this family of sealed, snap-action switches detects range of motion or the position of an object. These devices target automobile devices, including audio, interior lamp, accelerator- or break-pedal position, door latch, seat position, power mirror, trunk latch, sunroof, and shift levers. All of the switches handle 15A microloads and come in SPDT and SPST NC/SPST-NO configurations. Comprising the D2VW, D2SW, D3HW, D2HJ, D2FW-G, and Z-55 switches, the series' prices range from 73 cents to $10.41 (10,000).

Omron Electronic Components, www.omron.com

Three analog switches/multiplexers have wide voltage ranges

Operating over a 2.7 to 12V voltage range for single supply or a ±2.7 to ±6V range for dual supply, the DG9051, DG9052, and DG9053 analog switches/multiplexers come in an eight-channel analog multiplexer, a dual four-channel analog multiplexer, and a triple two-channel SPDT analog switch, respectively. Targeting cell phones, communication systems, data-acquisition systems, automated test equipment, and automotive systems, the devices feature a 0.8 to 2V logic range when operating from a 5V power supply or dual ±5V power supplies and a 0.8 to 2.4V logic range when operating with a 12V power supply. Depending on the power-supply configuration, the devices have on-resistances as low as 30Ω, with guaranteed on-resistance matching as low as 5Ω.



These analog switches/multiplexers cost 86 cents (1000).

Vishay, www.vishay.com

DPDT switch targets WiMax- and mesh-network applications

The GaAs (gallium-arsenide) MASWSS0184 DPDT high-power switch maximizes system-linearity performance and reduces dc power consumption. The device suits 802.16 WiMax- and mesh-network applications requiring 1-dB compression of 40-dBm handling, 1-dB typical insertion loss, and 30-dB isolation. Available in a 3×3-mm PQFN package, the MASWSS0184 is ROHS (reduction-of-hazardous-substances)-compliant and costs $2.25 (10,000).

M/A-Com, www.macom.com

Low-voltage analog switches target wireless-audio applications

Available in six-, 10-, and 16-pin options, these low-voltage analog switches suit high-current switching of audio signals in portable and wireless applications with low operating voltages. The NLAS5223-MNR2G dual-SPDT switch features a 0.35Ω on-resistance in a 2.6×1.8×0.75-mm QFN-16 package. The NLAS5223MNR2G single-SPDT switch features a 0.35Ω on-resistance in a 1.4×1.8×0.75-mm QFN-10 package. The LNAS5123MNR2G SPDT features a 1Ω on-resistance in a 1.2×1×0.75-mm DFN-6 package. The six-, 10-, and 16-pin devices cost 56, 67, and 97 cents (10,000), respectively.

On Semiconductor, www.onsemi.com

productroundup

EDA TOOLS

Simulator upgrade features RF-budget analysis

Upgrades for the analog RF VSS (visual-system simulator) include an RF-budget-analysis application, assisting users in deriving component specifications. The upgrades include an elastic buffer for faster simulations with multirate capability, a one-step signal generator for generator-test signals, and an intelligent receiver allowing changes at the transmitter end to eliminate potential design errors in the receiver. Targeting RF-IC designs, the simulator includes RF models in the designs' voltage domain. Dedicated system-engineering tools include RF cascade measurements for yield-analysis performance, impedance mismatch for monitoring VSWR (voltage-standing-wave ratio), and a fixed-point library. An autocompensation-filter phase rotation reduces bit-error-rate simulation time, and backward/forward propagation automatically adjusts the data rate.

Applied Wave Research Inc, www.appwave.com

Verification IP divides into three categories

Targeting use in the ZeBu emulation platform, this catalog of peripheral-verification IP (intellectual-property) models divides into synthesizable memory models, transactors, and hardware bridges. Memory modules replicate real memory modules in SDR, DDR, DDR2, and DIMM DRAM synthesizable models, as well as in NAND flash-memory models. The devices support memory uploading/downloading and reading/writing for each cell at runtime for interactive design debugging. Transactors interface a testbench written in C/C++/SystemC/SystemVerilog. They include the following protocols: PCI Express with one, two, four, or eight lanes; 10/100/1-Gbit Ethernet; Ethernet controller; LCD; JTAG; UART; keypad; keyboard; and mouse. A memory transactor extends the design memory to the pc RAM and supports MHz access. For compliance testing of standard protocols, the hardware bridges interface a physical peripheral to a mapped device under test, executing at a fraction of real-time speeds. Bridges are available for PCI/PCI-X and PCI Express with one-, two-, or four-lane protocols. The ZeBu Vertical Solution Catalog costs $5000 for a one-year, term-based license.

EVE, www.eve-team.com

INTEGRATED CIRCUITS

Programmable converter has 14 channels

Claiming improved accuracy and reliability of touch controls in handheld devices, the AD7142 programmable, 14-channel, 16-bit capacitance-to-digital converter operates from a 2.7 to 3.3V supply. Features include automatic environment compensation and the ability to perform calibration digitally on-chip and with SPI or I²C compatible interfaces. Peripherals include a 1-mA, full-power mode, a 2-μA shutdown current, and the ability to trade off output rate and power. Available in a 5×5-mm LFCSP-32 package, the AD7142 costs $1.09. AD7142 evaluation boards cost $199.

Analog Devices, www.analog.com

Processor IC provides FireWire connectivity

Targeting complex recording and mixing environments, BeBoB 3.1, running on the vendor's DM1500 processor IC, provides 80 audio channels at 96 kHz or 128 channels at 48 kHz. With the same processing capabilities as the DM-1500, the DM1100 processor IC also features 12 I/O channels at 192 kHz and enables FireWire audio systems requiring a 12-channel device. Both products come in bundled platforms, incorporating the processor IC and BeBoB firmware stack. The DM1100 combined firmware/processor platform costs $15 (1000), and the DM1500 firmware/processor platform costs $29 (1000).

BridgeCo, www.bridgeco.net

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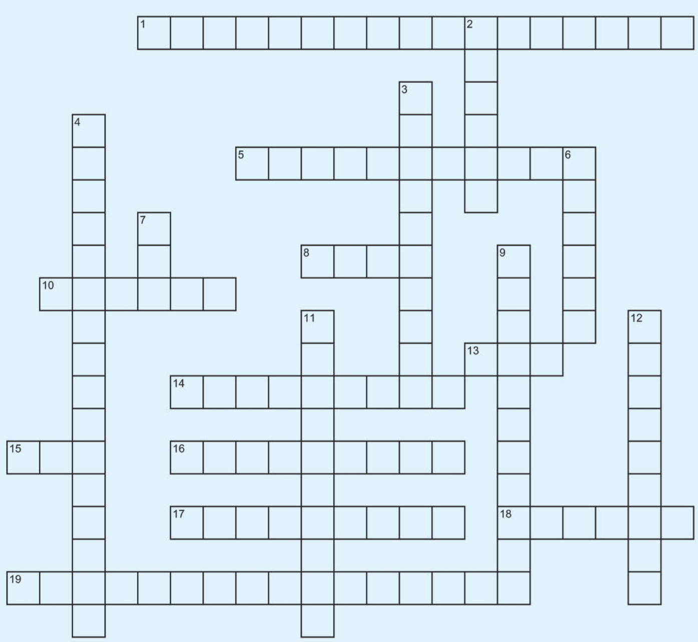

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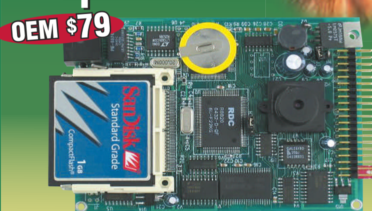

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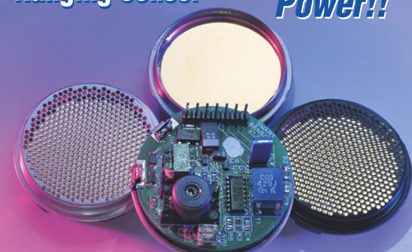

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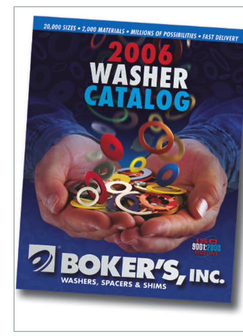

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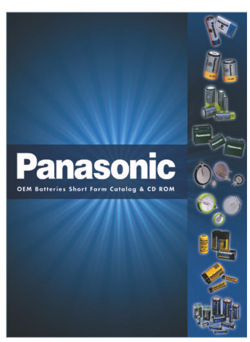

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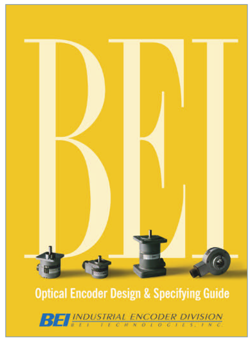

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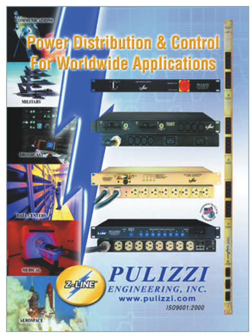

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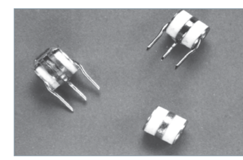

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STATS June 2000 introduction price: less than $300 / Total sales: 0

Kerbango Internet Radio was simply ahead of its time

When Kerbango introduced its Internet Radio in 2000, it was clear that broadband connections would ultimately make streaming media mainstream. Kerbango was the first to try to make the experience akin to using a consumer radio or boom box as opposed to requiring a PC. The company even planned the Kerbango Tuning Service, which would streamline the process of finding radio stations or other streaming-audio sources on the Internet. The concept was sufficiently compelling that 3Com reportedly paid $80 million to buy the start-up before killing the product in 2001.

Kerbango was too early for several reasons. Semiconductor technology simply couldn't yield such a product for $300 in 2000, despite the fact that the design was based on royalty-free Linux. Moreover, it required an Ethernet connection, and that factor defeated the portability angle. Despite a number of prototypes at trade shows, Kerbango never shipped the product to the public. But the concept lives on in products from Netgear, D-Link, Roku Labs, and others that range from less than $100 to approximately $500. Users can move today's offerings to the extent of their WiFi networks and can play radio and music from services such as Rhapsody and Musicmatch.—by Maury Wright

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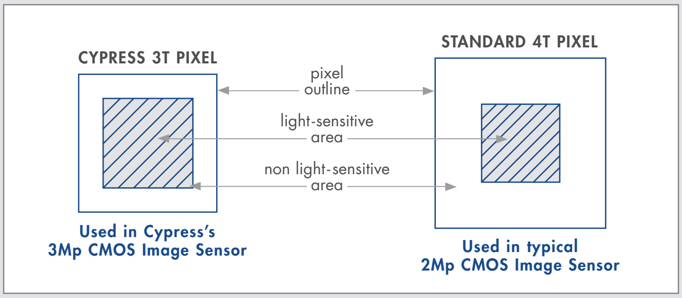

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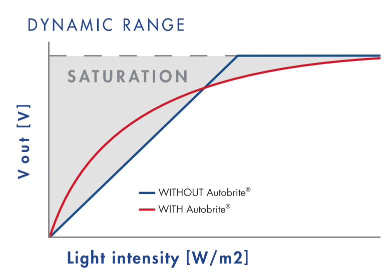

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